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Technical Specification

**Transmission and Multiplexing (TM);
Integrated Services Digital Network (ISDN) basic rate access;
Digital transmission system on metallic local lines**

Reference

RTS/TM-06017-1

Keywords

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Contents

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Foreword

This Technical Specification (TS) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

The present editorial update does improve the safety related provisions in the document.

1 Scope

The present document covers the characteristics and parameters of a digital transmission system at the network side of the NT1 to form part of the access digital section for the Integrated Services Digital Network (ISDN) basic rate access using echo cancellation method.

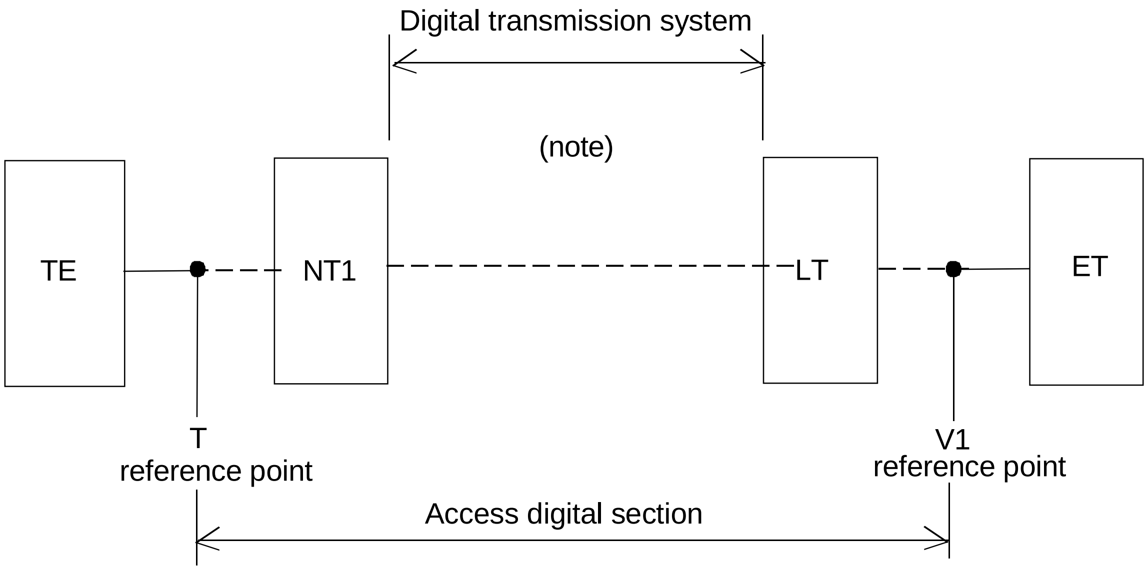
The present document specifies support for:

- full duplex; and

- bit sequence independent,

transmission of two B-channels and one D-channel as defined in ITU-T Recommendation I.412 [12] and the supplementary functions of the access digital section defined in ETR 001 [7].

The line codes of systems specified in the present document are 2B1Q (2 Binary 1 Quaternary) and MMS 43-code (Modified Monitoring State 43-code). Systems using a 2B1Q line code are covered in annex A. Systems using a MMS line code are covered in annex B. Only one of the line codes has to be realized in a transmission system. Figure 1 shows the boundaries of the digital transmission system in relation to the access digital section.



NOTE: In the present document, digital transmission system refers to a line system using metallic local lines. The use of one intermediate regenerator (REG) may be required.

Figure 1: Access digital section and transmission system boundaries

The concept of the access digital section is used in order to allow a functional and procedural description and a definition of the network requirements.

NOTE: The reference points T and V_1 are not identical and therefore the access digital section is not symmetric.

The concept of a digital transmission system is used in order to describe the characteristics of an implementation, using a specific medium, in support of the access digital section.

1.1 Objectives

Considering that the access digital section between the local exchange and the customer is one key element of the successful introduction of ISDN into the network, the following requirements for the specification have been taken into account:

- to operate on existing 2-wire unloaded lines, open wires being excluded;

- the objective is to achieve 100 % cable fill for ISDN basic access without pair selection, cable rearrangements or removal of Bridged Taps (BTs);
- the objective to be able to extend ISDN basic access provided services to the majority of customers without the use of regenerators. In the remaining few cases, special arrangements may be required;
- coexistence in the same cable unit with most of the existing services like telephony and voice band data transmission;
- various national regulations concerning Electro-Magnetic Compatibility (EMC) should be taken into account;
- power feeding from the network under normal or restricted modes via the basic access to be provided;
- the capability to support maintenance functions to be provided.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] ETSI ETS 300 012 (1998): "Integrated Services Digital Network (ISDN); Basic user-network interface; Layer 1 specification and test principles".

[2] ETSI ETS 300 019 (1994): "Equipment Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment".

[3] ETSI ETS 300 047-5 (1992): "Integrated Services Digital Network (ISDN); Basic access - safety and protection; Part 5: Interface I_b - protection".

[4] ETSI ETS 300 297 (1995): "Integrated Services Digital Network (ISDN); Access digital section for ISDN basic access".

[5] ETSI ETS 300 386-1 (1994): "Equipment Engineering (EE); Telecommunication network equipment; Electro-Magnetic Compatibility (EMC) requirements; Part 1: Product family overview, compliance criteria and test levels".

[6] ETSI EN 300 386-2 (V1.1): "Electromagnetic compatibility and Radio spectrum Matters (ERM); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements; Part 2: Product family standard".

[7] ETSI ETR 001 (1990): "Integrated Services Digital Network (ISDN); Customer access maintenance".

[8] ETSI EN 60950: “Safety of information technology equipment including electrical business equipment.".

[9] ITU-T Recommendation G.117 (1996): "Transmission aspects of unbalance about earth".

[10] ITU-T Recommendation G.821 (1996): "Error performance of an international digital connection operating at a bit rate below the primary rate and forming part of an integrated services digital network".

[11] ITU-T Recommendation G.823 (1993): "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".

[12] ITU-T Recommendation I.412 (1988): "ISDN user-network interfaces - Interface structures and access capabilities".

[13] ITU-T Recommendation K.17 (1988): "Tests on power-fed repeaters using solid-state devices in order to check the arrangements for protection from external interference".

[14] ITU-T Recommendation K.20 (1996): "Resistibility of telecommunication switching equipment to overvoltages and overcurrents".

[15] ITU-T Recommendation K.21(1996): "Resistibility of subscriber's terminal to overvoltages and overcurrent".

[16] Council Directive 89/336/EEC of 3 May 1989 on the approximation of the laws of the Member States relating to electromagnetic compatibility.

[17] ETSI ETR 080 (1996): "Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines".

[18] ETSI EG 201 212: “Electrical Safety; Classification of interfaces for equipment to be connected to telecommunication networks."

3 Abbreviations

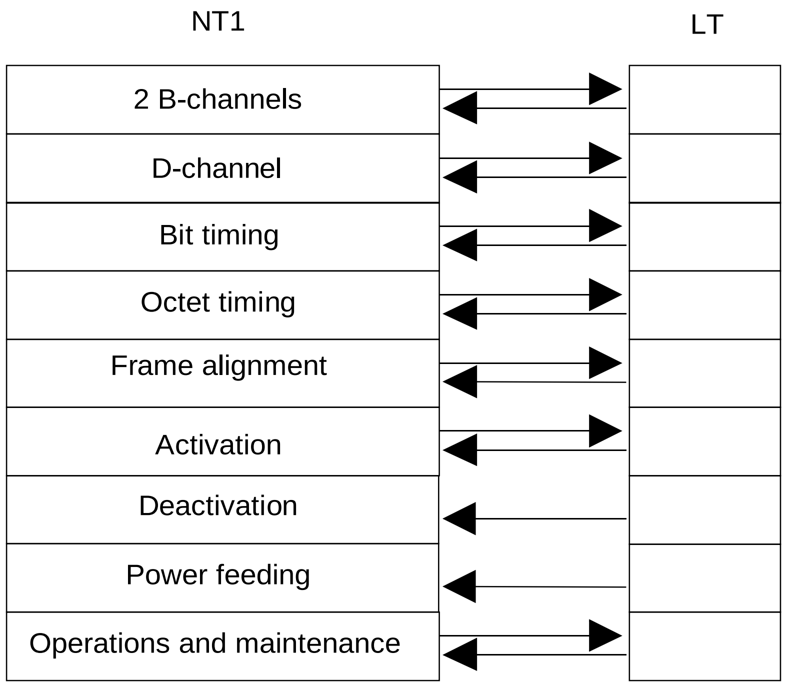
For the purposes of the present document, the following abbreviations apply:

2B1Q	2 Binary, 1 Quaternary
A/D	Analogue to Digital
AC	Alternating Current
AIB	Alarm Indicator Bit
BER	Bit Error Rate
BT	Bridged Tap
CCP	Cross Connection Point
CRC	Cyclic Redundancy Check
CSO	Cold-Start-Only
DC	Direct Current
DLL	Digital Local Line
DSL	Digital Subscriber Line
DTS	Digital Transmission System
EC	Echo Canceller
ECH	Echo Cancellation Hybrid
EMC	ElectroMagnetic Compatibility
EOC	Embedded Operations Channel
ET	Exchange Termination
FE	Failure Element
FEBE	Far End Block Error
FW	Frame Word
IFW	Inverted Frame Word
ISDN	Integrated Services Digital Network
LCL	Longitudinal Conversion Loss
LT	Line Termination
MDF	Main Distribution Frame
MMS	Modified Monitoring State
NEXT	Near End Crosstalk
NIB	Network Indicator Bit
NT	Network Termination
NTM	NT1 Test Mode
ppm	parts per million
PSL	Power Sum Loss
REG	Regenerator
rms	root mean squared

SAI	S/T-interface-Activity Indicator
SDP	Subscriber Distribution Point
TE	Terminal Equipment
UI	Unit Interval
UNI	User Network Interface
UOA	DLL-Only-Activation

4 Functions

Figure 2 shows the functions of the digital transmission system on metallic local lines.



NOTE: The optional use of one regenerator shall be foreseen.

Figure 2: Functions of the digital transmission system

4.1 B-channel

This function provides, for each direction of transmission, two independent 64 kbit/s channels for use as B-channels (as defined in ITU-T Recommendation I.412 [12]).

4.2 D-channel

This function provides, for each direction of transmission, one D-channel at a bit rate of 16 kbit/s, (as defined in ITU-T Recommendation I.412 [12]).

4.3 Bit timing

This function provides bit (signal element) timing to enable the receiving equipment to recover information from the aggregate bit stream. Bit timing for the direction NT1 to LT shall be derived from the clock received by the NT1 from the LT.

4.4 Octet timing

This function provides 8 kHz octet timing for the B-channels. It shall be derived from the frame alignment.

4.5 Frame alignment

This function enables the NT1 and the LT to recover the time division multiplexed channels.

4.6 Activation from LT or NT1

This function restores the Digital Transmission System (DTS) between the LT and NT1 to its normal operational status. Procedures required to implement this function are described in clause 8.

Activation from the LT may apply to the DTS only or to the DTS plus the customer equipment. In case the customer equipment is not connected, the DTS can still be activated (see note in subclause 4.9).

4.7 Deactivation

This function is specified in order to permit the NT1 and the regenerator (if it exists) to be placed in a low power consumption mode or to reduce intrasystem crosstalk to other systems. The procedures and exchange of information are described in clause 8. This deactivation should be initiated only by the exchange (ET).

4.8 Power feeding

This function provides for remote power feeding of one regenerator (if required), NT1 and restricted mode power feeding at the T reference point.

NOTE: The general power feeding strategy, given in clause 10, may not be applicable for extremely long local lines. In such cases, specific power feeding methods (e.g. use of batteries in the NT1 or local power feeding of the NT1) may be applied. The specific methods are outside the scope of the present document.

4.9 Operations and maintenance

This function provides the recommended actions and information described in ETR 001 [7].

The following categories of functions have been identified:

- maintenance command (e.g. loopback control in the regenerator or the NT1);
- maintenance information (e.g. line errors);
- indication of fault conditions;
- information regarding power feeding in NT1.

NOTE: The functions required for operations and maintenance of the NT1 and one regenerator (if required) and for some activation/deactivation procedures are combined in one transport capability to be transmitted along with the 2B+D channels. This transport capability is named the C_L channel.

5 Transmission medium

5.1 Description

The transmission medium over which the digital transmission system is expected to operate, is the local line distribution network.

A local line distribution network employs cables of pairs to provide services to customers.

In a local line distribution network, customers are connected to the local exchange via local lines.

A metallic local line is expected to be able to simultaneously carry bidirectional digital transmission providing ISDN basic rate access between LT and NT1.

To simplify the provision of ISDN basic access, a digital transmission system shall be capable of satisfactory operation over the majority of metallic local lines without requirement of any special conditioning. Maximum penetration of metallic local lines is obtained by keeping ISDN requirements at a minimum.

In the following, the term Digital Local Line (DLL) is used to describe a metallic local line that meets minimum ISDN requirements.

5.2 Minimum ISDN requirements

a) No loading coils;

b) No open wires;

c) When bridged taps (BTs) are present, the following rules apply:

- maximum number of BTs: 2;
- maximum BT length: 500 m.

NOTE: A BT is an unterminated twisted pair section bridged across the line.

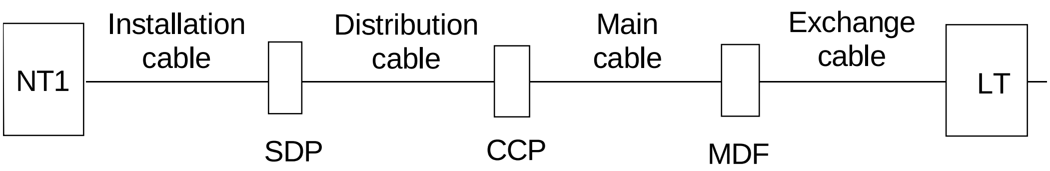
5.3 DLL physical characteristics

In addition to satisfying the minimum ISDN requirements, a DLL is constructed of one or more cable sections that are spliced or interconnected together.

The distribution or main cable is structured as follows:

- cascade of cable sections of different diameters and lengths;
- one or more BTs may exist at various points in feeder and distribution cables.

A general description is shown in figure 3 and typical examples of cable characteristics are given in table 1.



Points of interconnection:
MDF: Main Distribution Frame
CCP: Cross Connection Point (or splice)
SDP: Subscriber Distribution Point

Figure 3: DLL physical model

Table 1: Cable characteristics

	Exchange cable	Main cable	Distribution cable	Installation cable
Wire diameter (mm)	0,5; 0,6; 0,32; 0,4	0,3... 1,4	0,3... 1,4	0,4; 0,5; 0,6; 0,8; 0,9; 0,63
Structure	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ or TP or UP
Maximum number of pairs	1 200	2 400 (0,4 mm) 4 800 (0,32 mm)	600 (0,4 mm)	2 (aerial) 600 (in house)
Installation		underground in ducts or aerial	underground or aerial	aerial (drop) in ducts (in house)
Capacitance (nF/km at 800 Hz)	55... 120	25... 60	25... 60	35... 120
Wire insulation	PVC, FRPE	PE, paper pulp	paper, PE, Cell PE	PE, PVC

TP:	Twisted Pairs	PE:	Polyethylene
SQ:	Star Quads	PVC:	Polyvinylchloride
UP:	Untwisted Pairs	Pulp:	Pulp of paper
L:	Layer	Cell PE:	Cellular Foam Polyethylene
B:	Bundles (units)	FRPE:	Fire Resistant PE

NOTE: This table is intended to describe the cables presently installed in the local loop.

5.4 DLL characteristics

The transmitted signal will suffer impairment due to crosstalk, impulsive noise and the non-linear variation with frequency of DLL characteristics.

5.4.1 Principal characteristics

The principal electrical characteristics are:

- insertion loss (X), limited to 36 dB at 40 kHz for the system described in annex A and to 32 dB at 40 kHz for the system described in annex B;
- group delay, limited to 80 μs at 40 kHz;
- characteristic impedance, comprising real and negative imaginary parts, both of which vary non-linearly with frequency.

NOTE: The main reason for the difference of the value X for the two line systems is the system defined in annex B has a lower output power (peak voltage at output port), which provides lower signal to noise ratio against the adjusted noise level provided at the input port during performance tests.

5.4.2 Crosstalk

Crosstalk noise, in general, is due to finite coupling loss between pairs sharing the same cable, especially those pairs that are physically adjacent. Finite coupling loss between pairs causes a vestige of the signal flowing on one DLL (disturber DLL) to be coupled into an adjacent DLL (disturbed DLL). This vestige is known as crosstalk noise.

Near-End Crosstalk (NEXT) is assumed to be the dominant type of crosstalk.

Intrasystem NEXT or self NEXT results when all pairs interfering with each other in a cable carrying the same digital transmission system.

Intersystem NEXT results when pairs carrying different digital transmission systems interfere with each other. Definition of intersystem NEXT is not part of the present document.

Intrasystem NEXT noise coupled into a disturbed DLL from a number of DLL disturbers is represented as being due to an equivalent single disturber DLL with a coupling loss versus frequency characteristic known as Power Sum Loss (PSL). Its value is 50 dB at 40 kHz and decreases by 15 dB/decade with frequency.

5.4.3 Unbalance about earth

The DLL shall have finite balance about earth. Unbalance about earth is described in terms of Longitudinal Conversion Loss (LCL). Worst case value is 45,5 dB at 40 kHz decreasing with 5 dB/decade with frequency.

5.4.4 Impulse noise

The DLL will have impulse noise resulting from other systems sharing the same cables as well as from other sources. The design-requirement is an impulsive noise corresponding to figure 4.

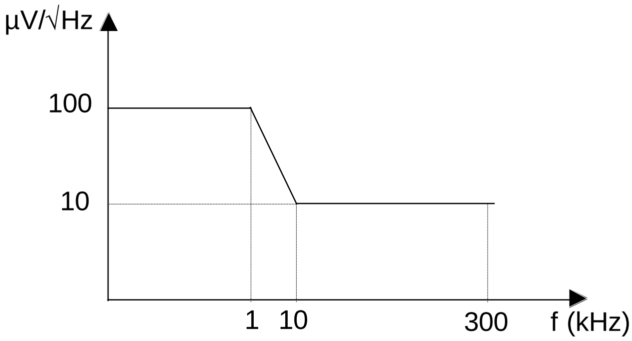


Figure 4: Impulse noise

5.4.5 Micro interruptions

A micro interruption is a temporary line interruption due to external mechanical activity on the copper wires constituting the transmission path, for example, at the cable splice. Splices can be hand made wire to wire junctions, and during cable life oxidation phenomena and mechanical vibrations can induce micro interruptions at these critical points.

The effect of a micro interruption on the transmission system can be a failure of the digital transmission link, together with a failure of the power feeding (if provided) for the duration of the micro interruption.

The objective is that the presence of a micro interruption of specified maximum length shall not deactivate the system, and the system shall activate if it has deactivated due to a longer interruption.

The system shall be able to perform an activation if deactivating after interruptions longer than 10 ms.

6 System performance

6.1 Performance requirements

Performance limits for the access digital section are specified in ITU-T Recommendation G.821 [10]. The DTS performance shall be such that these performance limits are met. For the purpose of conformance, a DTS is required to meet the specific laboratory performance tests that are defined in the following subclauses.

The defined performance tests cover several aspects:

- the performance of the system, when activated, with several test loops and noise injected;
- to allow reduced test time where appropriate;
- the ability of the system to activate successfully even with a noise injected, which may result in a degraded performance when activated.

For the latter item, the activation time may be greater than the limits defined in ETS 300 297 [4], for those tests where the expected error performance may be below 10^{-7}, but activated status shall be reached in all tests.

6.1.1 System performance with Regenerators (REGs)

If enhanced transmission range is required then a REG may be inserted between the LT and the NT. The LT - REG - NT combination shall be expected to meet the same BER and latency targets as a normal (non regenerated) link.

The REG may be inserted at any convenient intermediate point in the loop providing that:

a) the overall insertion loss (X) of the loop without the REG is < 1,8 X dB;

b) the REG is located within 0,9 X dB of the LT (see figure 5).

There may be further restrictions in the line length due to power feeding.

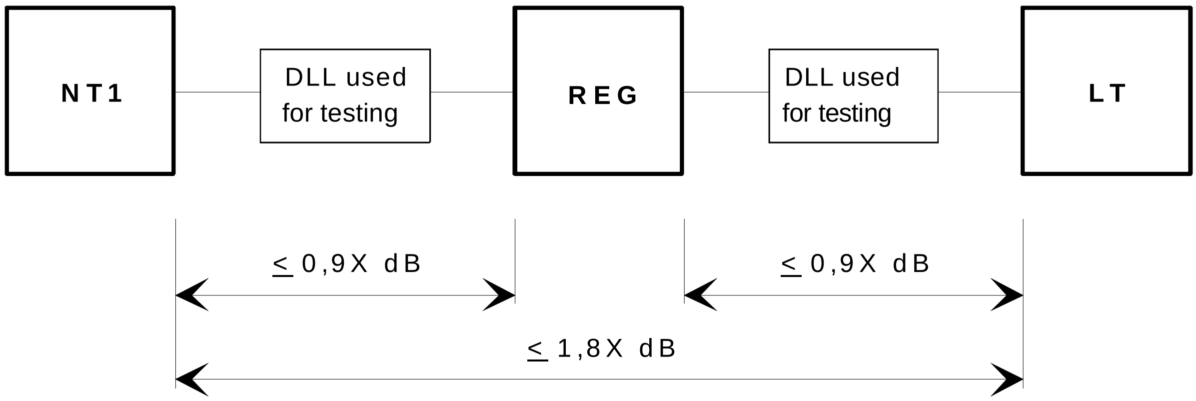


Figure 5: Access digital section with REG

6.2 Performance measurements

Laboratory performance measurement of a particular digital transmission system requires the following preparations:

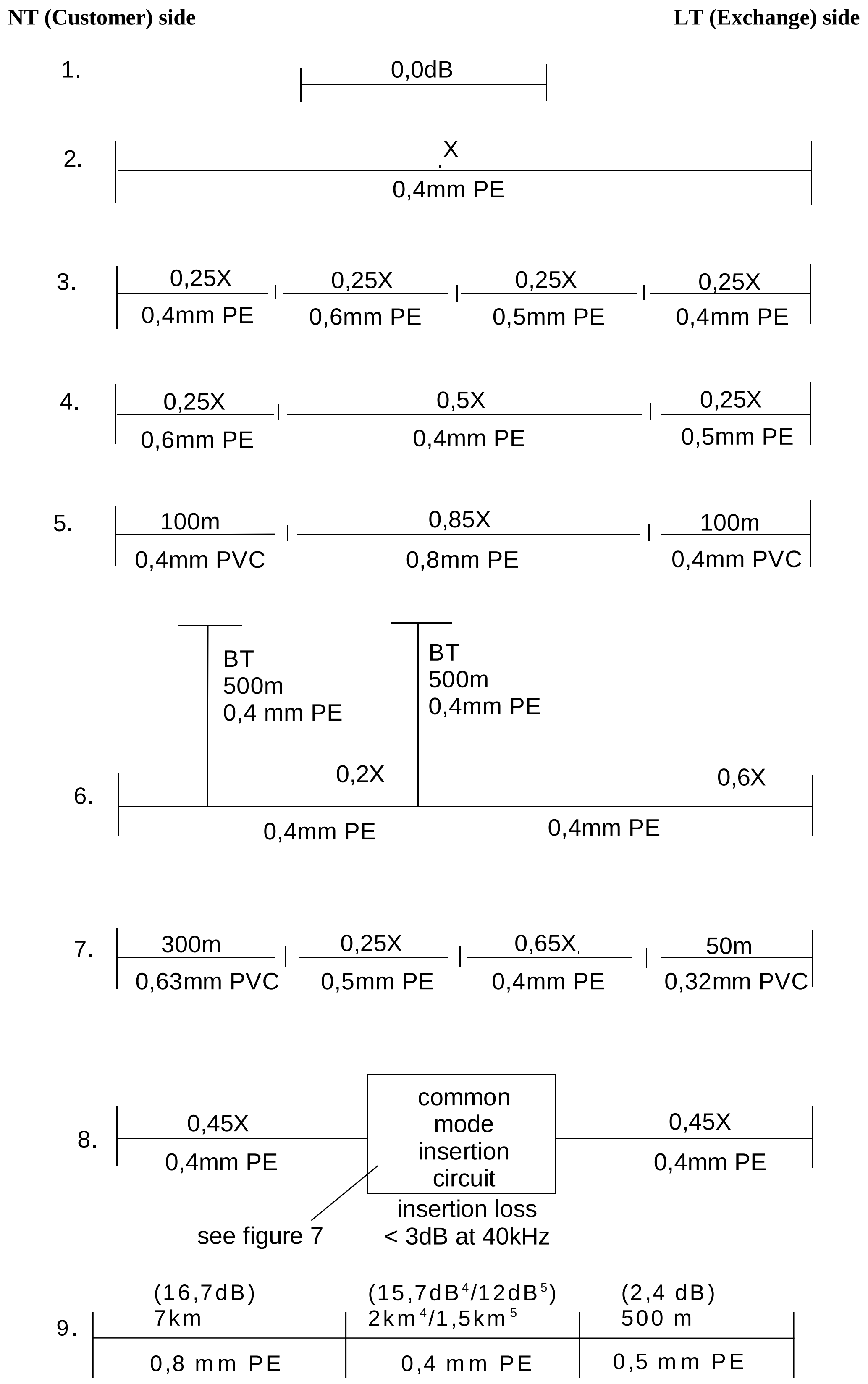
a) definition of a number of DLL models to represent physical and electrical characteristics encountered in local line distribution networks;

b) simulation of the electrical environment caused by impulsive noise and finite crosstalk coupling loss to other pairs in the same cable;

c) specification of laboratory performance tests to verify that the performance limits referred to in subclause 6.1 are met.

6.2.1 DLL physical models

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in figure 6.



NOTE 1: The value of X (insertion loss) is 36 dB at 40 kHz for the system described in annex A and 32 dB at 40 kHz for the system described in annex B.

NOTE 2: Due to mismatches and BTs, the total DLL attenuation differs from the sum of the attenuation of the parts.

NOTE 3: Attenuation of separate sections is measured with 135 Ω termination.

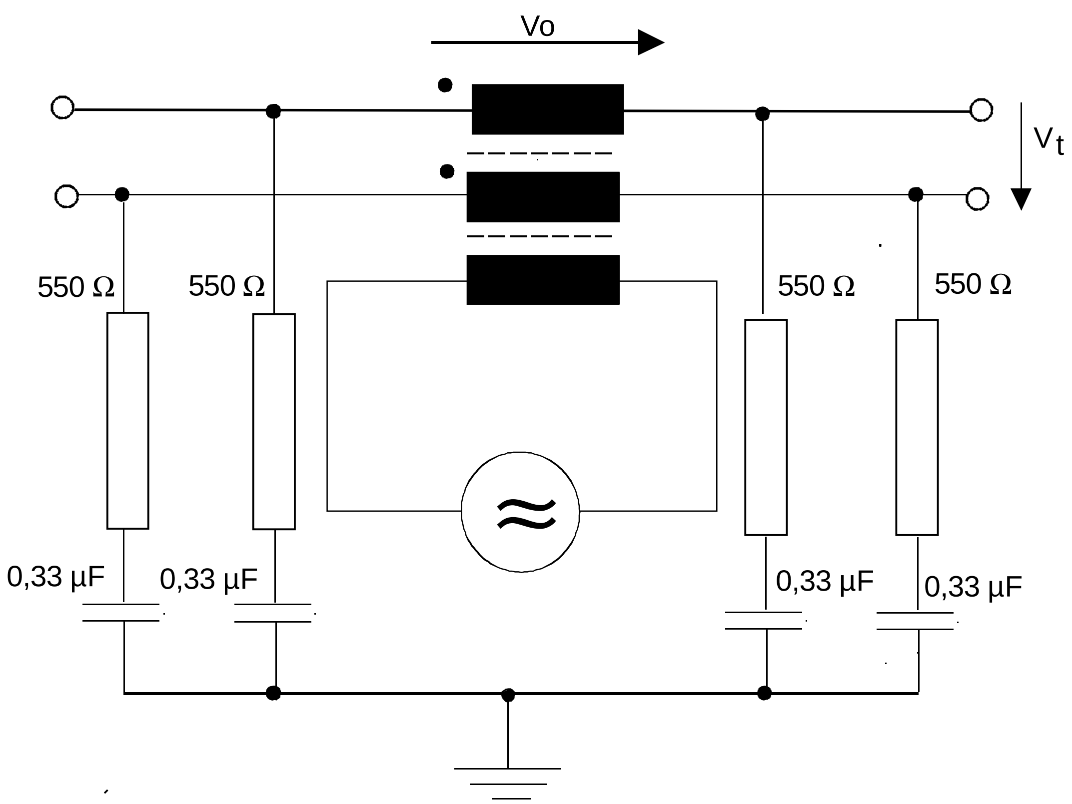
NOTE 4: Based on 36 dB overall insertion loss at 40 kHz for the system described in annex A.

NOTE 5: Based on 32 dB overall insertion loss at 40 kHz for the system described in annex B.

Figure 6: DLL physical models for laboratory testing

A brief description of the intention of the DLL physical models (shown in figure 6) used for laboratory testing is given:

1) void;
2) general loop; to verify operation on loops with reduced length this loop is also used in steps of 200 m between 0 m and maximum length; the loop causes a relevant increase of impedance at loop-lengths above 1 km;
3) multiple impedance changes equally divided over the cable length, causing multiple echoes;
4) average cable with some impedance changes; low impedance at NT side; high impedance at LT side;
5) extremely long, low impedance cable with impedance changes close to NT and LT; causing maximum delay;
6) cable with bridged taps;
7) multiple impedance changes; large changes close to NT and LT side; PVC cable represents in-house cabling;
8) common mode insertion test loop; test loop with extra low impedance at the NT (customer) end, which will stress the NT transceiver;
9) loop to stress the input impedance at the NT1 end.



NOTE 1: The minimum return loss of the terminated circuit shall be equal to the minimum return loss of the system.
NOTE 2: The minimum longitudinal conversion loss V_o/V_t shall be 80 dB at 50 Hz decreasing with 20 dB/decade up to 1 kHz. By this, the transversal voltage is negligible against shaped noise.

Figure 7: Common mode insertion circuit for DLL No. 8

The basic parameters of the types of cable used in the test loops are given in table 2.

More detailed test cable characteristics are given in annex C.

The test loops and artificial cable parameters include worst case examples as well as those more typical of a local network. They are chosen to provide the wide range of different echoes and distortions which may occur in European networks.

Table 2: Cable parameters at low frequencies (1 kHz)

Artificial cable type	C' (between wires)	R' (loop resistance)	L'
0,32 mm PVC	120 nF/km	420 Ωkm	650 µH/km
0,40 mm PVC	120 nF/km	270 Ω/km	650 µH/km
0,40 mm PE	45 nF/km	270 Ω/km	680 µH/km
0,50 mm PE	25 nF/km	172 Ω/km	680 µH/km
0,60 mm PE	56 nF/km	120 Ω/km	700 µH/km
0,63 mm PVC	120 nF/km	110 Ω/km	635 µH/km
0,80 mm PE	38 nF/km	68 Ω/km	700 µH/km
NOTE: For abbreviations see table 1.			

6.2.2 Intrasystem crosstalk

Crosstalk is dominated by impulsive noise.

6.2.3 Impulse noise modelling

6.2.3.1 Types of impulsive noise

Two classes of impulsive noise signals are used for testing:

a) shaped noise.

The impulsive noise in local network lines as relevant for the digital transmission system, with power feeding provided over this line, can be best represented by flat white noise from 10 kHz to 300 kHz with a level of 10 µV/√Hz. The signal amplitude increases below 10 kHz with 20 dB per decade down to 1 kHz.

This shaped noise shall be created by:

- 8 192 defined amplitude-values, stored in a memory;
- read out with a clock rate of 1 310 720 Hz, resulting to a noise signal composed of 4 096 sinusoidal signals of n x 160 Hz.

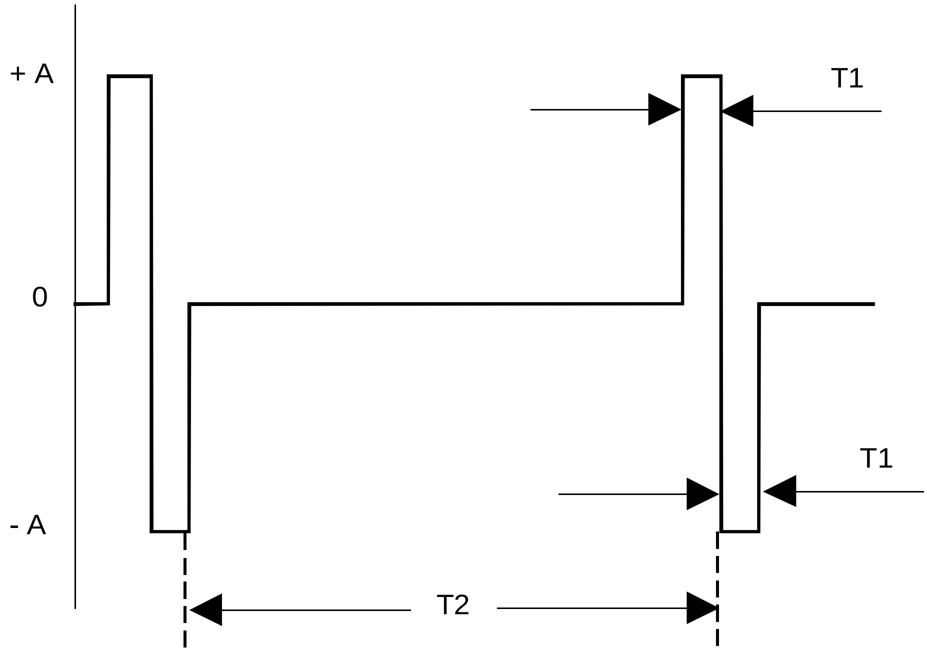
Table 3: Spectral density

Spectrum line n	Frequency range	Amplitude
1 to 6	0 kHz to 1 kHz	U
7 to 62	1 kHz to 10 kHz	Decrease with 20 dB/dec
63 to 1 875	10 kHz to 300 kHz	U/10
1 876 to 4 096	> 300 kHz	Zero

Phase relation for crestfactor 5:

$$\phi_n = \left(\pi x INT \left(\frac{n^3 - n^2}{1{,}5x4096} \right) \right) MOD(2\pi)$$

b) a particular waveform, as represented in figure 8.



A = peak level, set to 100 mV

T1 = pulse width, set to 50 µs

T2 = period >> T1, set to 500 ms

Figure 8: Waveform to simulate impulse noise

6.2.3.2 Measurement arrangement

Figure 9 shows the arrangement for testing with both impulse noise signals.

The coupling impedance shall be 4 kΩ ± 10 % in the frequency range of 1 kHz to 300 kHz.

The signal is calibrated towards 67,5 Ω.

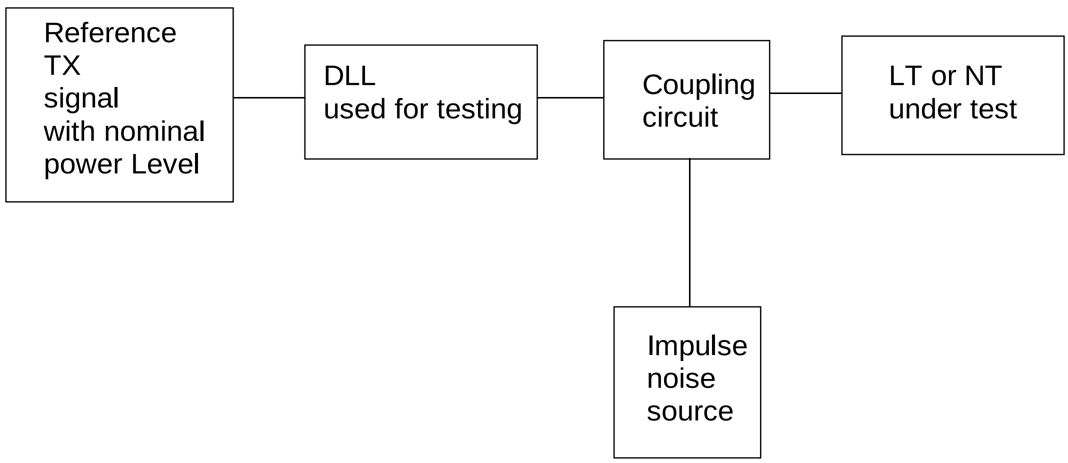


Figure 9: Impulse noise simulation and testing

6.2.4 Performance tests

All tests shall start from the deactivated status of the system.

6.2.4.1 TEST 1

Test sequence:

NOTE: The noise value is referenced to 10 µV/√Hz (= 0 dB) in the frequency range between 10 kHz and 300 kHz.

Table 3.A

Test	Loop	Noise	BER
a	2	+2,5 dB	$< 10^{-4}$
b	3	+2,5 dB	$< 10^{-4}$
c	3 reversed	+2,5 dB	$< 10^{-4}$
d	4	+2,5 dB	$< 10^{-4}$
e	4 reversed	+2,5 dB	$< 10^{-4}$
f	6	+2,5 dB	$< 10^{-4}$
g	6 reversed	+2,5 dB	$< 10^{-4}$
h	7	+2,5 dB	$< 10^{-4}$
i	7 reversed	+2,5 dB	$< 10^{-4}$
j	9	+2,5 dB	$< 10^{-4}$
k	loop of tests a...j with largest Bit Error Rate (BER - see note 1) with value X reduced by 10 dB	+10,5 dB	$< 10^{-4}$
l	loop 1	+10,5 dB	$< 10^{-4}$
m	2 loops of tests a...k with the largest BER (see note 1)	values of test a to k with the largest BER (see note 1) reduced by 2,5 dB and with jitter added as defined for the relevant system in annex A or B	$< 10^{-7}$
n	loop 5	0 dB	$< 10^{-7}$
o	loop of tests m or n with the largest BER (see note 1) with value X increased by 4 dB	no noise	$< 10^{-8}$
p	step loop 2 in steps of 200 m in the range from 200 m up to maximum loop length	+2,5 dB	$< 10^{-4}$
NOTE 1: If no errors are detected, loop 3 and 3 reversed shall be used for this test. NOTE 2: Measuring time for BER $< 10^{-7}$: 60 minutes; Measuring time for BER $< 10^{-4}$: 30 seconds; Measuring time for BER $< 10^{-8}$: 180 minutes (another 180 minutes if failed).			

Tests a...j (loop 2...7, 9) are performed to find out the most critical loop for each implementation in a short time.

Test k and l are performed to test improvement of noise with reduced DLL-loss.

Test m and n is performed to test the most critical situation for BER $< 10^{-7}$ with nominal noise.

Test o is performed to test intrinsic noise of the implementation.

Test p is performed to test the ability of handling different loop-length.

6.2.4.2 TEST 2

Test 2 shall use loop 2 and inserting the pulse signal given in figure 7 (representing noise peaks with high amplitudes) with the characteristics T1 = 50 µs, T2 = 500 ms, A = 100 mV, measurement time period > 10s, BER $< 10^{-3}$.

6.2.4.3 TEST 3

Test 3 shall test the common mode rejection capability of an implementation. Test loop 8 shall be used with a common mode triangle signal of 50 Hz with a voltage of 15 V rms for the first harmonic (25,5 Vp). The 21st harmonic (1 050 Hz) shall be 53 to 56 dB below the level of the first harmonic and the BER of the system shall be $< 10^{-7}$.

6.2.5 Micro interruption test

A system shall tolerate a micro interruption up to t ms, when stimulated with a repetition interval of T=5 s. The value of t is limited to 10 ms for a system described in annex A (2B1Q). No requirement for micro interruptions is made for systems described in annex B (4B3T). No requirement for micro interruptions is applicable for systems deployed before January 1, 1998.

A test configuration for laboratory susceptibility tests is described in figure 10.

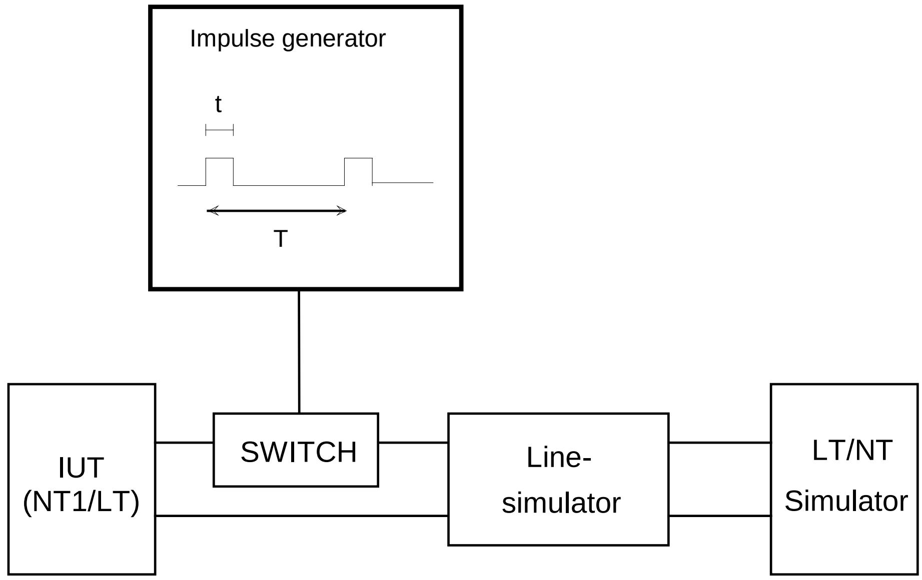


Figure 10: Laboratory test configuration for measuring micro interruption susceptibility

6.3 Unbalance about earth

6.3.1 Longitudinal conversion loss

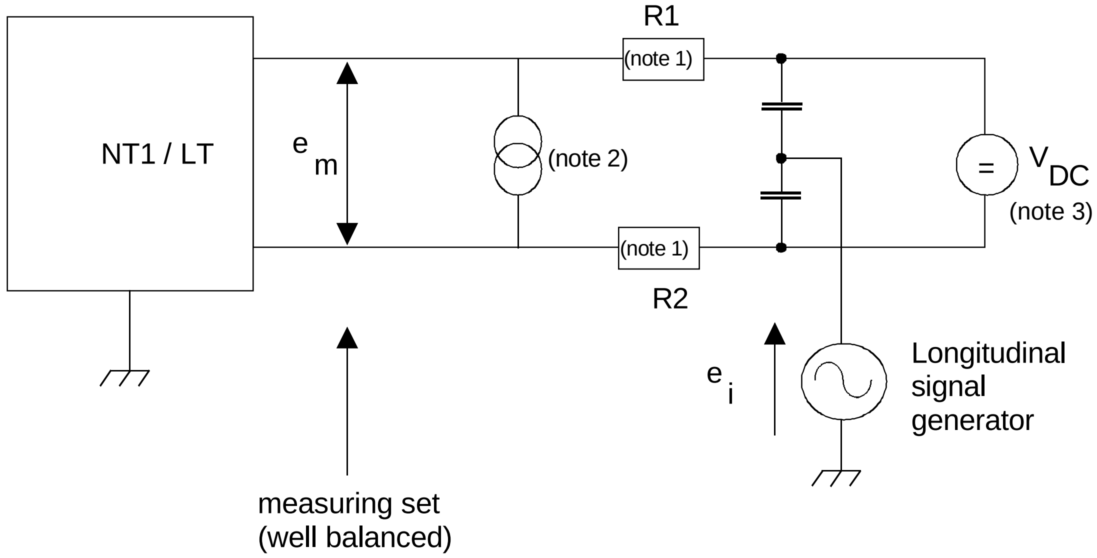
The longitudinal conversion loss (LCL, referring to ITU-T Recommendation G.117 [9]) is given by:

$$LCL = 20\log\frac{e_i}{e_m}dB$$

where e_i is the applied longitudinal voltage referenced to the building ground; e_m is the resultant metallic voltage appearing across either a 135 Ω or a 150 Ω termination, depending on the system as given in annex A or annex B.

The balance shall be as described in figure A.15 (135 Ω termination) or figure B.7 (150 Ω termination).

Figure 11 defines a measurement method for longitudinal conversion loss. For direct use of this test configuration, measurement should be performed with the NT1 powered up but inactive (no transmitted signal, i.e. driving 0 volts).



NOTE 1: These resistors shall be matched: R1 = R2 = RT/2; R1:R2 = 1 ± 0,1 %.

NOTE 2: For LT-test only.

NOTE 3: For NT1 and REG test only.

NOTE 4: During REG-Test, each wire at the side which is not under test shall be connected to ground by a terminating impedance having the value of RT/2 in series with a capacitance of 0,33 µF.

RT: The nominal driving point impedance at the interface towards the NT1, REG and LT.

Values for RT for the relevant system are given in annex A or annex B. The characteristics of the power sink and source are dependant on the power feeding implementation.

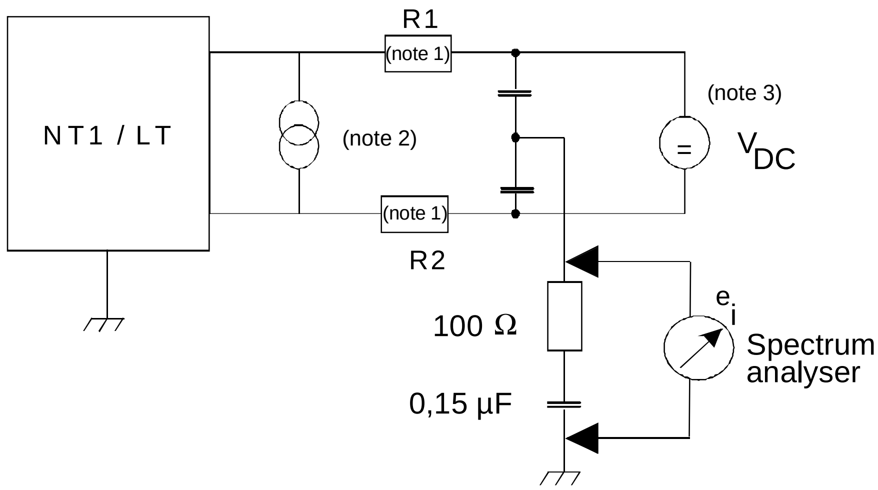
Figure 11: Measurement method for longitudinal conversion loss

6.3.2 Longitudinal output voltage

The longitudinal component of the output signal shall have an rms voltage, in any 4 kHz equivalent bandwidth averaged in any 1 second period, < -50 dBV (provisional) over the frequency range 100 Hz to 150 kHz. Compliance with this limitation shall be required with a longitudinal termination having an impedance of 100 Ω in series with 0,15 µF nominal.

For frequencies above 150 kHz, the relevant EMC requirements shall be taken into consideration (see subclause 11.4).

Figure 12 defines a measurement method for longitudinal output voltage. For direct use of this test configuration, the NT1 should be able to generate a signal in the absence of a signal from the LT and vice versa. The ground reference for these measurements shall be the building ground.



NOTE 1: These resistors shall be matched: R1 = R2 = RT/2; R1:R2 = 1 ± 0,1 %
NOTE 2: For LT-test only.
NOTE 3: For NT1-test only.
NOTE 4: During REG-Test, each wire at the side which is not under test shall be connected to ground by a terminating impedance having the value of RT/2 in series with a capacitance of 0,33 µF.

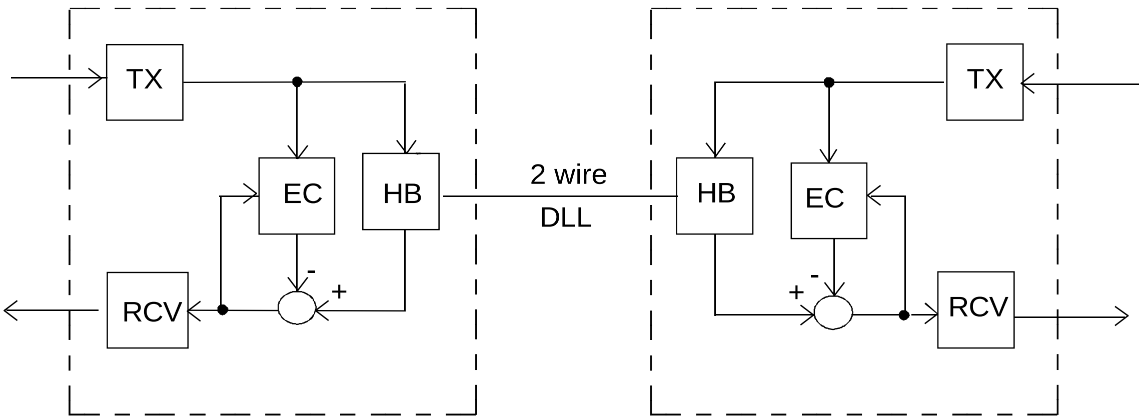
RT: The nominal driving point impedance at the interface towards the NT1, REG and LT.

Values for RT for the relevant system are given in annex A or annex B. The characteristics of the power sink and source are dependant on the power feeding implementation.

Figure 12: Measurement method for longitudinal output voltage

7 Transmission method

The transmission system provides for duplex transmission on 2-wire metallic local lines. Duplex transmission shall be achieved through the use of Echo Cancellation Hybrid (ECH). With the ECH method, illustrated in figure 13, the Echo Canceller (EC) produces a replica of the echo of the transmitted signal that is subtracted from the total received signal. The echo is the result of imperfect balance of the hybrid and impedance discontinuities in the line.



TX: Transmitter
RCV: Receiver
EC: Echo Canceller
HB: Hybrid

Figure 13: ECH method functional diagram

8 Activation/deactivation

8.1 General

The functional capabilities of the activation/deactivation procedure are specified in ETS 300 297 [4] and the transmission system shall meet the requirements specified therein. In particular, it shall make provision to convey the signals defined in ETS 300 297 [4], which are required for the support of the procedures.

8.2 Physical representation of signals

The signals used on the digital transmission system are system dependent and can be found in annexes A and B.

9 Operation and maintenance

9.1 Operation and maintenance functions

The functions are defined in ETS 300 297 [4].

9.2 C_L channel

9.2.1 C_L channel definition

This channel is conveyed by the digital transmission system in both directions between LT and NT1 via a possible regenerator. It is used to transfer information concerning operation, maintenance and activation/deactivation of the digital transmission system and of the access digital section.

Even though some of these functions have an optional status, the C_L channel shall have the capability to convey the necessary information to perform the function.

9.2.2 C_L channel requirements

The functions to be supported by the C_L channel are given in annex A and annex B.

9.3 Metallic loop testing

The requirements for NT1 and REG regarding metallic loop testing are described in subclause 10.8.

10 Power feeding

10.1 General

This clause deals with power feeding of the NT1, one regenerator (if required) and the provision of power to the User Network Interface (UNI) according to ETS 300 297 [4] under normal and restricted conditions.

When activation/deactivation procedures are applied, power down modes at the NT1, regenerator (if required) and the LT are defined.

10.2 Power feeding functions

For power feeding three functions can be distinguished:

- power feeding of the REG;
- power feeding of the NT1;
- power feeding of the user network interface.

10.2.1 Power feeding of the REG

Remote power feeding of the REG from the network is preferred.

10.2.2 Power feeding of the NT1

Remote powering of the NT1 from the network is preferred under all conditions.

NOTE: The general power feeding strategy may not be applicable for extremely long local lines. In those cases, specific power feeding methods (e.g. use of batteries in the NT1 or local power feeding of the NT1) may be applied. Those specific methods are outside the scope of the present document.

10.2.3 Power feeding of the user network interface

Power feeding of the UNI is described in ETS 300 012 [1].

According to ETS 300 012 [1], power feeding of restricted mode power to the UNI from the network during restricted mode conditions should be considered.

The provision of restricted mode power is not related to the state of the NT1 (e.g. activated or deactivated).

10.3 DLL resistance

This parameter is a particular subject of the individual local network and, therefore, out of the scope of the present document. Its maximum value depends on the LT output voltage, the power consumption of the NT1 and regenerator (if required) and the power feeding arrangement of the user network interface.

10.4 Wetting current

The feeding current to the NT1 and regenerator (if required) results in a Direct Current (DC) through the DLL. To maintain a minimum wetting current, the NT1 and the side of the REG directed towards the LT shall sink a current of at least 200 µA in its operating voltage range.

10.5 LT aspects

10.5.1 Feeding voltage from the LT

No unique remote power feeding voltage to be provided by the LT can be defined because of the following reasons:

- different national safety requirements;
- different DLL planning rules;
- the optional use of regenerators.

A number of feeding voltage ranges is defined for different applications.

The minimum and maximum voltages from those ranges at the output of the LT are given in table 4.

Table 4: Voltage ranges

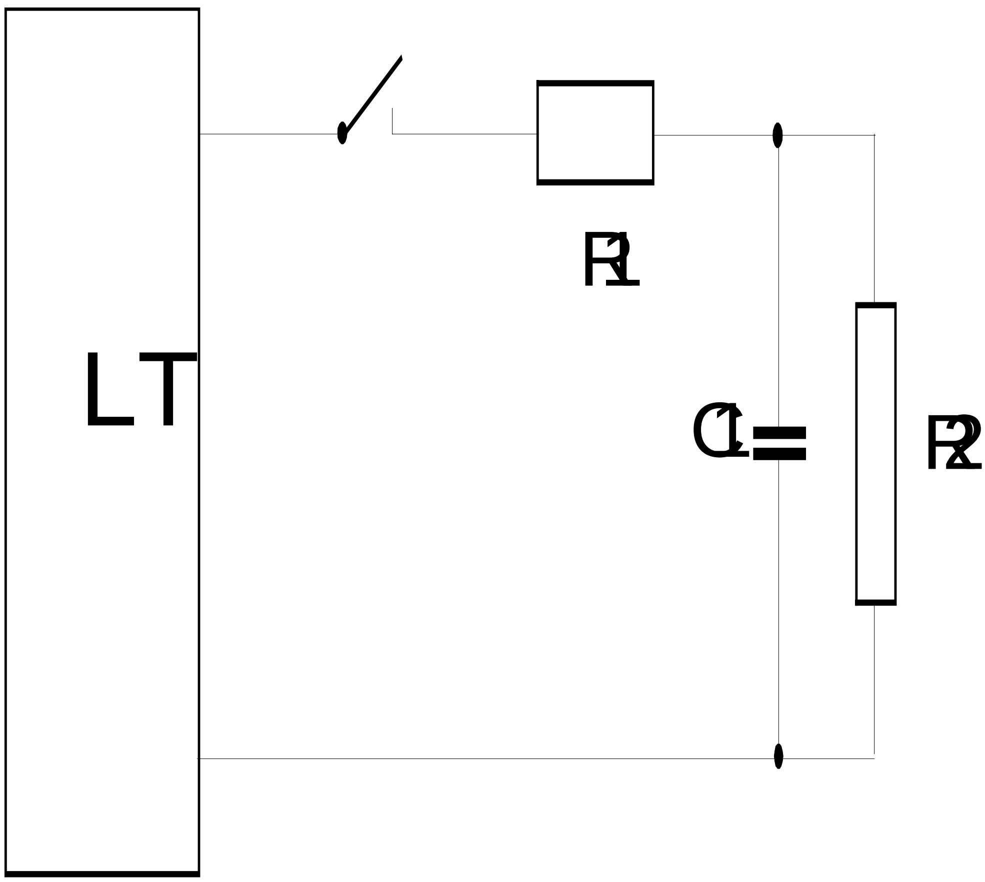
Minimum (V)	Maximum (V)
51	69
66	70
91	99
90	110
105	115

10.5.2 Dynamic power feeding requirements

The values given in this subclause represent currently used practice of testing dynamic power feeding behaviour.

1) Sources with a fixed current limitation between 40 mA and 55 mA shall provide a current of ≥ X mA for at least 1,5 s before switch-off. The value of X depends upon the feeding voltage range and shall be in accordance with table 5.

2) Sources without current limitation or with a current limitation greater than 55 mA shall not switch-off when the test circuit given in figure 14 is connected.



NOTE: Additional requirements may be needed to guarantee operation under all working conditions.

Figure 14: LT power source test load

Table 5: Values of components for LT power source test loads according to figure 14

Voltage range	R1 (Ω)	C1 (µF)	R2 (Ω)	X (mA)
51 to 69 V	100	200	5 000	45
66 to 70 V	900	200	1 000	40
91 to 99 V	1 000	400	3 000	45
90 to 110 V	1 000	400	3 000	40
105 to 115 V	1 000	400	3 000	40

10.5.3 LT requirements for the reset of NT1 and REG

The LT shall provide for reset function a voltage below 5 V for at least 2 seconds when measured over a load of 100 kΩ connected to the LT terminals.

When equipment is used which is deployed before January 1, 1998 and which cannot meet the 2 seconds requirement, this equipment may use up to 4 seconds.

10.6 Power requirements of NT1 and regenerator

10.6.1 Power requirements of NT1

10.6.1.1 Static requirements

a) Active state without powering of user-network interface or when normal mode power is supplied to the network: ≤ 500 mW.

b) Active state including restricted mode powering of the user-network interface as defined in ETS 300 012 [1]: ≤ 1 100 mW. This value includes a possible overload or short circuit condition at the user-network interface.

c) Deactivated state without powering of the UNI or when normal power is supplied: ≤ 120 mW.

While deactivated and in restricted power conditions, the NT1 shall be able to supply 420 mW into the S interface within the operation voltage range of the S interface.

NOTE: In case of a NT1 with optional maintenance functions, the power consumption may be increased.

10.6.1.2 Dynamic requirements

The values given in this subclause represent currently used practice of testing dynamic power feeding behaviour.

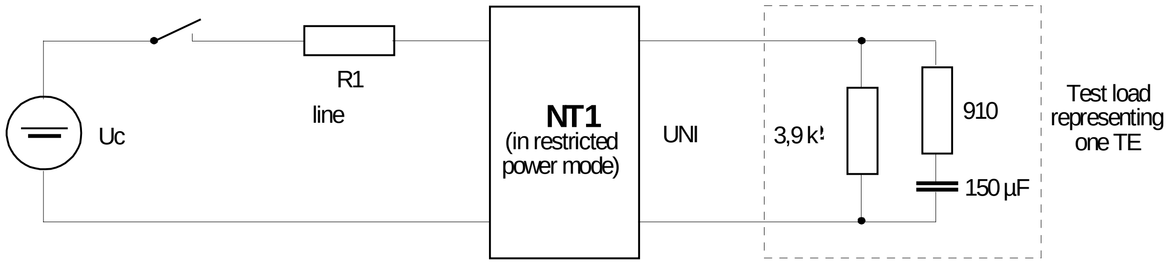
1) Tests shall be carried out with the test circuit given in figure 15 without REG simulation and in figure 16 with REG simulation respectively under one of the two test conditions:

   a) Awake signal and feeding voltage shall appear at the same point in time on the line;

   b) Awake signal appears first and then the feeding voltage is switched on.

2) 1,5 s after switch-on of the feeding voltage the current drawn by the test circuit including REG from the voltage source shall be below X mA where X shall be according to table 6 or table 7 respectively.

3) When the voltage at the NT exceeds for a first time 28 V, this voltage limit shall be maintained further on and shall not go below 28 V again.

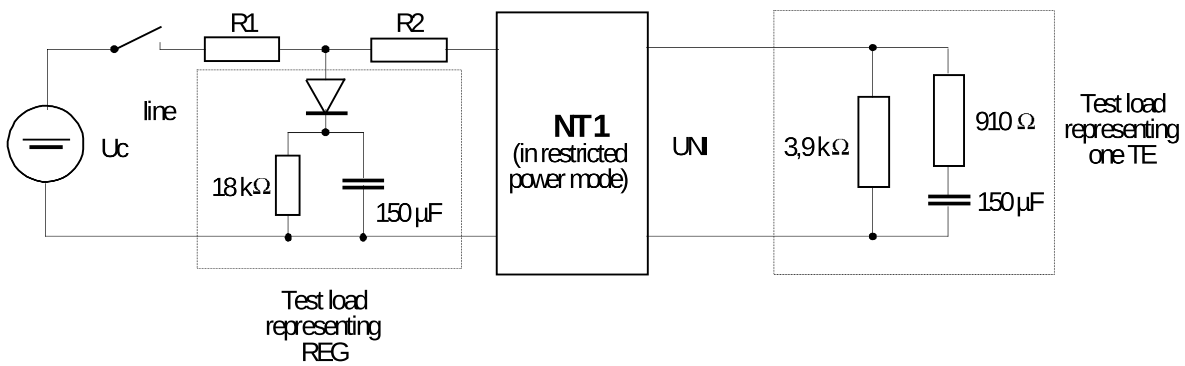


NOTE: U_C represents the lowest voltage of the voltage range and is current limited to the value X in table 6.

Figure 15: Test circuit for NT1 without REG simulation

Table 6: Values of components for NT1 power source test loads according to figure 15

Voltage range		R1 (Ω)	X (mA)
51 to 69 V	51 to 54 V	500	45
	54 to 69 V	600	45
66 to 70 V		900	40
91 to 99 V		1 000	45
90 to 110 V		1 000	40
105 to 115 V		1 000	40



NOTE 1: U_C represents the lowest voltage of the voltage range and is current limited to the value X in table 7.
NOTE 2: Additional requirements may be needed to guarantee operation under all working conditions.

Figure 16: Test circuit for NT1 with REG simulation

Table 7: Values of components for NT1 power source test loads according to figure 16

Voltage range	R1 (Ω)	R2 (Ω)	X (mA)
91 to 99 V	1 000	400	45
90 to 110 V	1 000	400	40
105 to 115 V	1 000	400	40
NOTE: For the use of a NT1+REG up to the maximum line resistance, the power consumption values as given in subclause 10.6.1 and/or 10.6.2 shall be reduced.			

10.6.2 Power requirement of regenerator

10.6.2.1 Static requirements

a) Active state: ≤ 1 000 mW.

b) Deactivated state: ≤ 180 mW.

c) Power off state (voltage at the REG lower than 45 V): the current drawn by the REG shall be ≤ 1 mA.

NOTE: For case a), the target value of 750 mW should be reached in the long term.

10.6.2.2 Dynamic requirements

The values given in this subclause represent currently used practice of testing dynamic power feeding behaviour.

The requirements that follow apply when the REG and the NT1 are powered from the line. Other powering scenarios (such as local powering) are possible.

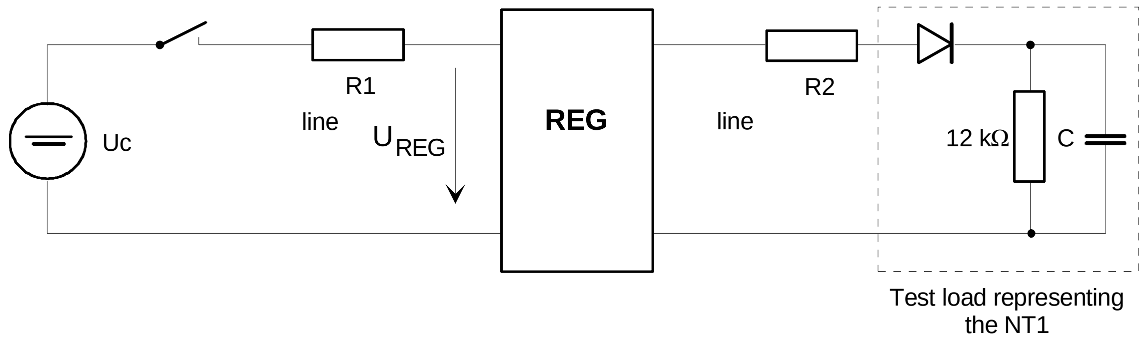
1) Tests shall be carried out with the test circuit given in figure 17 and one of the two test conditions:

   a) Awake signal and feeding voltage shall appear at the same point in time on the line;

   b) Awake signal appears first and then the feeding voltage is switched on.

2) 1,5 s after switch-on the feeding voltage the current drawn by the test circuit including REG as shown in figure 15 from the voltage source shall be below X mA where X shall be according to table 8.

3) When the voltage U_{REG} at the REG exceeds for a first time the voltage U_{REGmin}, this voltage limit shall be maintained further on and shall not go below U_{REGmin} again.



NOTE 1: U_C represents the lowest voltage of the voltage range and is current limited to the value X in table 8.
NOTE 2: Additional requirements may be needed to guarantee operation under all working conditions.

Figure 17: Test circuit for REG

Table 8: Values of components for LT power source test loads according to figure 17

Voltage range	U_{REGmin} (V)	R1 (Ω)	C (µF)	R2 (Ω)	X (mA)
51 to 69 V	Not applicable				
66 to 70 V	Not applicable				
91 to 99 V	50	1 000	150	400	45
90 to 110 V	60	1 000	150	400	40
105 to 115 V	60	1 000	150	400	40
NOTE: For the use of a NT1+REG up to the maximum line resistance the power consumption values as given in subclause 10.6.1 and/or 10.6.2 shall be reduced.					

10.6.3 Feeding voltage to the NT1

The minimum voltage at which the NT1 should work is 28 V.

Considering that the minimum voltage at the NT1 is depending on the remote powering voltage as well as the power consumption of the NT1 and REG, this voltage may be increased accordingly.

10.6.4 Voltage drop across the REG

The voltage drop between the LT-side and the NT-side of the REG shall be less than 2 V under all normal operation conditions.

10.6.5 Reset of NT1 and REG

The NT1 and the regenerator, independently from the operating condition such as feeding voltage, line resistance, active/deactivated state and power drawn by the user/network interface, shall enter a reset state (i.e. physical reset of the line transceiver) not later than 2 seconds after interruption of the remote current fed towards the NT or the REG respectively.

NT1 devices deployed before January 1, 1998, which cannot meet the 2 s requirement may use up to 4 s.

10.7 Current transient limitation

The rate of change of current drawn by the NT1 or regenerator from the network shall not exceed 1 mA/µs.

This is applicable only when initial powering of the NT1 has been completed.

10.8 DC and low frequency AC termination of NT1 and REG

Within 2 s after interruption of the remote current fed towards the NT or the REG respectively, the NT1 and the side of the REG directed towards the LT shall enter a high impedance state. This state shall be maintained as long as the voltage on the line stays below 18 V (DC + Alternating Current (AC) peak). In this state the leakage current shall be less than 10 µA and the capacitance shall be greater than 1 µF.

A guard time of at least 2 s between removing the remote power and applying a test voltage is necessary.

NT1 devices deployed before January 1, 1998, which cannot meet the 2 s requirement may use up to 4 s.

11 Environmental conditions

11.1 Climatic conditions

Climatograms applicable to the operation of NT1 and LT equipment in weather protected and non-weather protected locations can be found in ETS 300 019 [2]. The choice of classes is under national responsibility.

11.2 Safety

Requirements for safety are outside the scope of the present document. Safety standards are published by CENELEC.

NOTE 1: An exemple of such a CNELEC product safety standard is EN 60950 [8].

NOTE 2: For safety categories of interfaces, see ETSI guide EG 201 212 [18].

11.3 Overvoltage protection

For LT: Conform to ITU-T Recommendation K.20 [14].

For NT1: Conform to ITU-T Recommendation K.21 [15] and ETS 300 047-5 [3].

For REG: Conform to ITU-T Recommendation K.17 [13].

11.4 EMC

The EMC requirements are defined according to the equipment type and as described in EN 300 386-2 [6] or ETS 300 386-1 [5] as applicable.

NOTE: Additional EMC requirements may be imposed under EMC Directive (89/336/EEC [16]).

Annex A (normative): Definition of a system using 2B1Q line code

A.1 Line code

The line code shall be 2 Binary, 1 Quaternary (2B1Q). This is a 4-level code and is used without redundancy.

The bit stream entering the NT1 from the interface at reference point T (or entering the LT from the ET) shall be grouped into pairs of bits for conversion to quaternary symbols that are called **quats**. Figure A.1 shows the relationship of the bits in the B and D channels to quats. The B-channel and D-channel bits are scrambled before coding. M_1 through M_6 bits of the C_L channel are also paired, coded and scrambled in the same way.

Each successive pair of scrambled bits in the binary data stream is converted to a quaternary symbol to be output from the transmitters, as specified:

First Bit (Sign)	Second Bit (Magnitude)	Quaternary Symbol (Quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

At the receiver, each quaternary symbol is converted to a pair of bits by reversing the table, descrambled, and formed into a bit stream representing B and D channels and a C_L channel containing M bits for maintenance and other purposes. The bits in the B and D channels are properly placed by reversing the relationship in figure A.1.

A.2 Line baud rate

The line symbol rate shall be 80 kbaud.

A.2.1 NT1 clock tolerance

The tolerance of the free running NT1 clock shall be ± 100 ppm.

A.2.2 LT clock tolerance

The tolerance of the clock signal provided by the LT shall be ± 32 ppm with a frequency drift of $< 5 \times 10^{-7}$ per day.

A.2.3 REG clock tolerance

The tolerance of the free running REG clock shall be ± 100 ppm.

A.3 Frame structure

A frame shall be 120 quaternary symbols transmitted within a nominally 1,5 ms interval. Each frame contains a frame word, 2B+D data and C_L channel bits shown in figure A.2.

A.3.1 Frame length

The number of 2B+D slots in a frame shall be 12. Each slot shall contain 18 bits.

A.3.2 Bit allocation in direction LT to NT1

The bit allocation of the frames are shown in figures A.1 and A.2.

A.3.3 Bit allocation in direction NT1 to LT

The bit allocation of the frames are shown in figures A.1 and A.2.

Data	Time ----> B_1				B_2				D
Bit pairs	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q_5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where:

b_{11} = first bit of B_1 octet as received at reference point T;

b_{18} = last bit of B_1 octet as received at reference point T;

b_{21} = first bit of B_2 octet as received at reference point T;

b_{28} = last bit of B_1 octet as received at reference point T;

d_1d_2 = consecutive D-channel bits

(d_1 is first bit of pair as received at reference point T);

q_i = i^{th} quat relative to start of given 18-bit 2B+D data field.

NOTE: There are 12 2B+D 18-bit fields per 1,5 ms basic frame.

Figure A.1: 2B1Q encoding of 2B+D bit fields

←------------------------------ 1,5 ms ------------------------------→

FRAME	FW / IFW	12 x (2B+D)	CL

Function	Frame word	2B+D	Overhead
# Quats	9	108	3
Quat Positions	1-9	10-117	118-120
# Bits	18	216	6
Bit Positions	1-18	19-234	235-240

NOTE: Frames in the NT1 to network direction are offset from frames in the network to NT1 direction by 60 ± 2 quats.

Symbols and abbreviations:

quat	=	quaternary symbol = 1 baud.
-3, -1, +1, +3	=	symbol names.
2B+D	=	Customer data channels B_1, B_2 and D.
FW	=	Frame Word (9 symbol code).
	=	+3 +3 -3 -3 -3 +3 -3 +3 +3.
IFW	=	Inverted (or complementary) Frame Word.
	=	-3 -3 +3 +3 +3 -3 +3 -3 -3.
CL	=	M-channel bits, M_1-M_6.

Figure A.2: Frame structure of 2B1Q transmission system

A.4 Frame word

The Frame Word (FW) is used to allocate bit positions to the B, D, and C_L channels. It may also be used for baud synchronization.

A.4.1 Frame word in direction LT to NT1

The code for the FW in all frames except the first in a multiframe shall be:

FW = +3 +3 -3 -3 -3 +3 -3 +3 +3

The code for the FW of the first frame of a multiframe shall be an Inverted Frame Word (IFW):

IFW = -3 -3 +3 +3 +3 -3 +3 -3 -3

A.4.2 Frame word in direction NT1 to LT

See subclause A.4.1.

A.5 Frame alignment procedure

Unique frame alignment procedure is not specified. However, the time limits specified in clause A.10 shall be met.

A.6 Multiframe

To enable the allocation of the C_L channel bits over more than one frame, a multiframe is used. The start of the multiframe is determined by the IFW. The number of frames in a multiframe shall be 8.

A.6.1 Multiframe word in direction NT1 to LT

See subclause A.4.1.

A.6.2 Multiframe word in direction LT to NT1

See subclause A.4.1.

A.7 Frame offset between LT to NT1 and NT1 to LT frames

The NT1 shall synchronize transmitted frames with received frames (LT to NT1 direction). Transmitted frames shall be offset with respect to received frames by 60 ± 2 quaternary symbols (i.e. approximately 0,75 ms).

A.8 C_L channel

The C_L channel shall consist of the last three symbols (6 bits) in each basic frame of the multiframe.

A.8.1 Bit rate

The bit rate for the C_L channel shall be 4 kbit/s.

A.8.2 Structure

48 bits of a multiframe shall be used for the CL channel and are referred to as M bits.

24 bits per multiframe (2 kbit/s) shall be allocated to an embedded operations channel (EOC) which supports operations communications needs between the network and the NT1.

12 bits per multiframe (1 kbit/s) shall be allocated to a Cyclic Redundancy Check (CRC) function.

12 bits per multiframe (1 kbit/s) shall be allocated to other functions and spare bits as shown in figure A.3.

A.8.3 Protocol and procedures

The C_L channel functions (M bits) specified are based on the bit allocation for the multiframe defined in figure A.3.

		FRAMING	**2B+D**	**CL (overhead) bits M_1 - M_6**					
	Quat positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit positions	1-18	19-234	235	236	237	238	239	240
Multi frame #	Basic frame #	Frame word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
		LT to NT1							
A	1	IFW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	ACT	1	1
	2	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	DEA	1	FEBE
	3	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	1	CRC_1	CRC_2
	4	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	1	CRC_3	CRC_4
	5	FW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	1	CRC_5	CRC_6
	6	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	1	CRC_7	CRC_8
	7	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	UOA	CRC_9	CRC_{10}
	8	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	AIB	CRC_{11}	CRC_{12}
B,C,...									
		NT1 to LT							
1	1	IFW	2B+D	EOC_{a2}	EOC_{a2}	EOC_{a3}	ACT	1	1
	2	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	PS_1	1	FEBE
	3	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	PS_2	CRC_1	CRC_2
	4	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	NTM	CRC_3	CRC_4
	5	FW	2B+D	EOC_{a1}	EOC_{a2}	EOC_{a3}	CSO	CRC_5	CRC_6
	6	FW	2B+D	EOC_{dm}	EOC_{i1}	EOC_{i2}	1	CRC_7	CRC_8
	7	FW	2B+D	EOC_{i3}	EOC_{i4}	EOC_{i5}	SAI	CRC_9	CRC_{10}
	8	FW	2B+D	EOC_{i6}	EOC_{i7}	EOC_{i8}	1^*	CRC_{11}	CRC_{12}
2,3,...									

NOTE: 8 x 1,5 ms basic frames → 12 ms multiframe. NT1 to network multiframe delay offset from network to NT1 multiframe by 60 ± 2 quats (approximately 0,75 ms). All bits other than the FW are scrambled.

Symbols and abbreviations to figure A.3:

- ACT = activation bit (set to ONE during activation).
- AIB = alarm indication bit (ZERO indicates interruption).
- CRC = Cyclic Redundancy Check: covers 2B+D & M4:
  1 = most significant bit;
  2 = next most significant bit, etc.
- CSO = Cold-start-only bit (ONE indicates cold-start-only).
- DEA = deactivation bit (set to ZERO to announce deactivation).
- EOC = embedded operations channel:
  a = address bit;
  dm = data/message indicator;
  i = information (data/message).
- FEBE = far end block error bit (ZERO for errored multiframe).
- NTM = NT1 in test mode bit (ZERO indicates test mode).
- PS_1, PS_2 = power status bits (ZERO indicates power problems).
- quat = pair of bits forming quaternary symbol:
  s = sign bit (first) in quat;
  m = magnitude bit (second) in quat.
- SAI = S-activation indicator bit (optional, set = 1 for S/T activity).
- UOA = DLL-only-bit (optional, set = 1 to activate S/T).
- "1" = reserve bit for future definition; set = ONE.
- "1^*" = network indicator bit; reserved for network use, set = ONE.
- 2B+D = user data, bits 19-234 in basic frame.
- M = CL channel, bits 235-240 in basic frame.
- FW/IFW = frame word/inverted frame word, bits 1-18 in frame.

Figure A.3: 2B1Q multiframe technique and overhead bit assignments

A.8.3.1 Error monitoring function

A.8.3.1.1 Cyclic redundancy check

The CRC bits are the M_5 and M_6 bits in frames 3 through 8 of the multiframe. The CRC is an error detection code that shall be generated from the appropriate bits in the multiframe and inserted into the bit stream by the transmitter. At the receiver, a CRC calculated from the same bits shall be compared with the CRC value received in the bit stream. If the two CRCs differ, there has been at least one error in the covered bits in the multiframe.

A.8.3.1.2 CRC algorithms

The CRC code shall be computed using the polynomial:

$P(x) = x^{12} \oplus x^{11} \oplus x^3 \oplus x^2 \oplus x \oplus 1;$

where:

$\oplus$ = modulo 2 summation.

One method of generating the CRC code for a given multiframe is illustrated in figure A.4. At the beginning of a multiframe, all register cells are cleared. The multiframe bits to be covered by the CRC are then clocked into the generator from the left. During bits which are not covered by the CRC (FW, IFW, M_1, M_2, M_3, M_5, M_6), the state of the CRC generator is frozen and no change in state of any of the stages takes place. After the last multiframe bit to be covered by the CRC is clocked into REGISTER CELL 1, the 12 register cells contain the CRC code of the next multiframe. Between this point and the beginning of the next multiframe, the register cell contents are stored for transmission in the CRC field of the next multiframe. Notice that multiframe bit CRC1 resides in REGISTER CELL 12, CRC2 in REGISTER CELL 11, etc.

The ONEs and ZEROs from the interface at the T reference point, and corresponding bits from the network (across the V_1 reference point), shall be treated as ONEs and ZEROs, respectively, for the computation of the CRC.

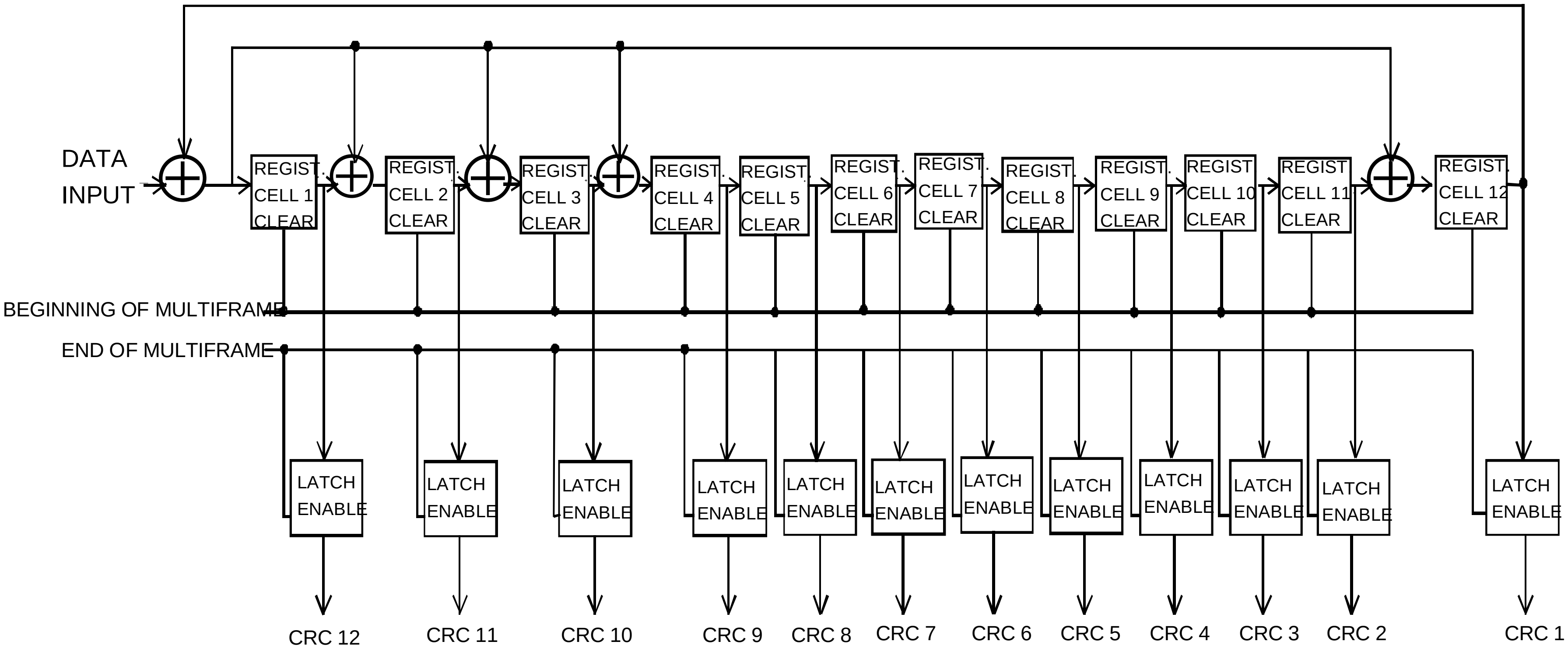


Figure A.4: CRC-12 generator

A.8.3.1.3 Bits covered by the CRC

The CRC bits shall be calculated from the bits in the D-channel, both B-channels, and the M_4 bits.

A.8.3.2 Other C_L channel functions

A number of transceiver operations and maintenance functions are handled by M_4, M_5, and M_6 bits in the multiframe. These bits are defined in subclauses A.8.3.2.1 to A.8.3.2.11. To reflect a change in status, a new value for M_4 bits shall be repeated in at least three consecutively transmitted multiframes.

A.8.3.2.1 Far end block error bit, mandatory

The Far End Block Error (FEBE) bits shall be the M_6 bits in the second basic frame of the multiframes transmitted by either transceiver. The FEBE bit shall be set to ONE if there are no CRC errors in the multiframe and ZERO if the multiframe contains a CRC error. The FEBE bit shall be placed in the next available outgoing multiframe and transmitted back to the originator. The FEBE bits may be monitored to determine the performance of the far end receiver.

A.8.3.2.2 The ACT bit, mandatory

The ACT bit is the M_4 bit in the first frame of multiframes transmitted by either transceiver. The ACT bit is used as a part of the start-up sequence to communicate readiness for layer 2 communication progress (see subclause A.10.1.5.2). If a loopback 2B+D is requested, the ACT Bit shall be set to ONE as a part of the loopback start-up sequence to communicate readiness to loopback data.

A.8.3.2.3 The DEA bit, mandatory

The DEA bit is the M_4 bit in the second frame of multiframes transmitted from the LT (see clause A.3 and figure A.3). The DEA bit is used by the LT to communicate to the NT1 its intention to deactivate (see subclause A.10.1.5.2).

A.8.3.2.4 NT1 power status bits

The M_4 bits in the second and third basic frames of multiframes transmitted by the NT1 (see figure A.3) are reserved for NTI power status indication; their use is optional. When not used, these bits shall be set to ONE in SN3 (see annex A1).

A.8.3.2.5 NT1 Test Mode (NTM) indicator bit

The M_4 bit in the fourth basic frame of multiframes transmitted by the NT1 to the network (see figure A.3) is reserved for NT1 test mode indication. This function is not used, the bit shall be set to ONE in SN3 (see annex A1).

A.8.3.2.6 Cold-Start-Only (CSO) bit

The M_4 bit in the fifth frame of the multiframe transmitted by an NT1 is reserved for cold-start-only indication. This function is not used, this bit shall be set to ZERO in SN3 (see annex A1).

A.8.3.2.7 DLL-Only-Activation (UOA) bit

The M_4 bit in the seventh basic frame of the multiframes transmitted by an LT is reserved for DLL-only activation; its use is optional. If this function is not used, this bit shall be set to ONE in SL2 and SL3 (see annex A1).

A.8.3.2.8 S/T-Interface-Activity-Indicator (SAI) bit

The M_4 bit in the seventh basic frame of the multiframes transmitted by an NT1 is reserved for S/T-interface-activity-indication; its use is optional. If this function is not used, this bit shall be set to ONE in SN3 (see annex A1).

A.8.3.2.9 Alarm Indicator Bit (AIB)

The M_4 bit in the eighth basic frame of the multiframes transmitted by the network towards the NT1 is reserved for the AIB. This function is not used, the AIB bit shall be set to ONE in SN3 (see annex A1).

A.8.3.2.10 Network Indicator Bit (NIB) for network use

The NIB bit shall be the M_4 bit in the eighth basic frame of multiframes transmitted by the NT1 towards the network. This function is not used, the NT1 shall always set this bit to ONE in SN3.

A.8.3.2.11 Reserved bits

All bits in M_4, M_5, and M_6 not otherwise assigned are reserved for future standardization. Reserved bits shall be set to ONE before scrambling.

A.8.3.3 Embedded Operations Channel (EOC) functions

24 bits per multiframe (2 kbit/s) shall be allocated to an EOC which supports operations communications needs between the network and the NT1.

A.8.3.3.1 EOC frame

The EOC frame shall be composed of 12 bits synchronized to the multiframe (see table A.1).

Table A.1: The EOC frame layout

Bits	3	1	8
Function provided	Address field	Data/message indicator	Info field

The three-bit address field may be used to address up to 7 locations. Only the specification of addresses of messages for the NT1 are within the scope of the present document. The additional addresses are for intermediate network elements where the system is used to extend access involving REG's and, e.g., carrier systems.

The detailed coding for the address of REGs or other intermediate elements can be found in annex A2.

The data/message indicator bit shall be set to ONE to indicate that the information field contains an operations message; it shall be set to ZERO to indicate that the information field contains numerical data. Up to 256 messages may be encoded in the information field.

Exactly two EOC frames shall be transmitted per multiframe consisting of all M_1, M_2, and M_3 bits (see figure A.3).

A.8.3.3.2 Mode of operation

The EOC protocol operates in a repetitive command/response mode. Three identical properly-addressed consecutive messages shall be received before an action is initiated. Only one message, under the control of the network, shall be outstanding (not yet acknowledged) on a complete basic access EOC at any one time.

The network shall continuously send an appropriately addressed message. In order to cause the desired action in the addressed element, the network shall continue to send the message until it receives three identical consecutive EOC frames from the addressed device that agree with the transmitted EOC frame. When the network is trying to activate an EOC function, autonomous messages from the NT1 will interfere with confirmation of receipt of a valid EOC message. The sending by the NT1 and receipt by the network of three identical consecutive properly addressed "Unable to Comply" messages constitutes notification to the network that the NT1 does not support the requested function, at which time the network may abandon its attempt.

The addressed element shall initiate action when, and only when, three identical, consecutive, and properly addressed EOC frames, that contain a message recognized by the addressed element, have been received. The NT1 shall respond to all received messages. The response should be an echo of the received EOC frame towards the network with two exceptions described below. Any reply or echoed EOC frame shall be transmitted in the next available returning EOC frame, which allows a processing delay of approximately 2,25 ms.

If the NT1 does not recognize the message (data/message bit set to ONE) in a properly addressed EOC frame, rather than echo, on the third and all subsequent receipts of that same correctly addressed EOC frame it shall return the "Unable to Comply" message in the next available EOC frame.

If the NT1 receives EOC frames with addresses other than its own address (000), or the broadcast address (111), it shall, in the next available EOC frame, return an EOC frame towards the network containing the "Hold State" message and its own address (the NT1 address, 000).

If a NT1, not implementing EOC data transfer functions, receives a data byte (data/message bit set to ZERO) in a properly addressed EOC frame, rather than echo on the third and subsequent receipts of that same correctly addressed EOC frame it shall return the "Unable to Comply" message in the next available EOC frame.

The protocol specification has made no provision for autonomous messages from the NT1.

All actions to be initiated at the NT1 shall be latching, permitting multiple EOC-initiated actions to be in effect simultaneously. A separate message shall be transmitted by the network to unlatch.

The transition of the transmission system through either RECEIVER RESET or FULL RESET states shall release all the outstanding EOC-controlled operations and reset the EOC processor to "return to normal" (unlatching all pending EOC commands).

A.8.3.3.3 Addressing

An NT1 shall recognize either of two addresses, an NT1 and a broadcast address. These addresses are as follows:

Table A.1A

Node	Address
NT1	000
Broadcast (all nodes)	111

A NT1 shall use the address 000 in sending the "Unable to Comply" message.

A REG or other intermediate elements shall use the address bit field values 1 to 6 (see subclause A.8.3.3.1).

A.8.3.3.4 Definition of required EOC functions

1) **Operate 2B+D Loopback:** This function directs the NT1 or REG to loopback the user-data (2B+D) bit stream towards the network. This loopback is transparent (see ETS 300 297 [4]).

2) **Operate B1-channel (or B2-channel) Loopback:** This function directs the NT1 or REG to loopback an individual B channel towards the network. The individual B-channel loopback can provide per-channel maintenance capabilities without totally disrupting service to the customer. This loopback is transparent (see ETS 300 297 [4]). The implementation and operation of the individual B-channel loopbacks is optional.

When a single B-channel is looped back, the setting of the ACT-bit shall not be changed because of the loopback (the ACT bit remains to be used to reflect the status of the TE as during normal operation). It is recommended that the ET management is not using the ACT bit, but to use the EOC channel to verify a successful single B-channel Loopback.

3) **Return to Normal:** The purpose of this message is to release all outstanding EOC-controlled operations and to reset the EOC processor to its initial state.

4) **Unable to Comply Acknowledgement:** This will be the confirmation that the NT1 or REG has validated the receipt of an EOC message, but that the EOC message is not in the menu of the NT1.

5) **Request Corrupt CRC:** This message requests the sending of corrupt CRCs towards the network until cancelled with Return to Normal.

6) **Notify of Corrupted CRC:** This message notifies the NT1 and/or REG that intentionally corrupted CRCs will be sent from the network until cancellation is indicated by Return to Normal.

7) **Hold State:** This message is sent by the network to maintain the NT1 EOC processor and any active EOC controlled operations in their present state. This message may also be sent by the NT1 towards the network to indicate that the NT1 has received an EOC frame with an improper address.

A.8.3.3.5 Codes for required EOC functions

Table A.2 shows the codes for each of the EOC functions defined in subclause A.8.3.3.4.

Table A.2: Messages required for command/response EOC mode

origin (o) & destination (d) & transfer (t)				
MESSAGE	**Message code**	**Network**	**NT1**	**REG**
Operate 2B+D Loopback	0101 0000	o	d	t/d
Operate B1-channel Loopback (note)	0101 0001	o	d	t/d
Operate B2-channel Loopback (note)	0101 0010	o	d	t/d
Request Corrupted CRC	0101 0011	o	d	t/d
Notify of Corrupted CRC	0101 0100	o	d	t/d
Return to Normal	1111 1111	o	d	t/d
Hold State	0000 0000	d/o	o/d	o/d/t
Unable to Comply Acknowledgement	1010 1010	d	o	t/o
NOTE: The use of B1 and B2 channel loopbacks is optional. However, the loopback codes are reserved for these functions.				

64 EOC messages have been reserved for non-standard applications in the following 4 blocks of 16 codes each (x is ONE or ZERO): 0100 xxxx, 0011 xxxx, 0010 xxxx, 0001 xxxx. Another 64 EOC message codes have been reserved for internal network use in the following 4 blocks of 16 codes each (x is ONE or ZERO): 0110 xxxx, 0111 xxxx,1000 xxxx, 1001 xxxx. All remaining codes not defined in table A.2 and not reserved for non-standard applications or for internal network use are reserved for future standardization. Therefore, 120 codes associated with the NT1 (000), and REG or other intermediate elements (001 to 110), and broadcast (111) addresses, are available for future definition; i.e. 256 total codes minus 8 defined codes from the table minus 64 codes for non-standard applications minus 64 codes for internal network use.

The reservation of codes for non-standard applications does not in any way endorse their use. Any use of such messages shall not interfere with the EOC protocol. An NT1/REG and an LT that support messages for non-standard applications may not function properly together.

A.9 Scrambling

The data stream in each direction of transmission shall be scrambled with a 23rd order polynomial (see figure A.5) prior to the insertion of FW.

In the LT-NT1 direction, the polynomial shall be:

- $1 \oplus x^{-5} \oplus x^{-23}$

where $\oplus$ = modulo 2 summation.

In the NT1-LT direction, the polynomial shall be:

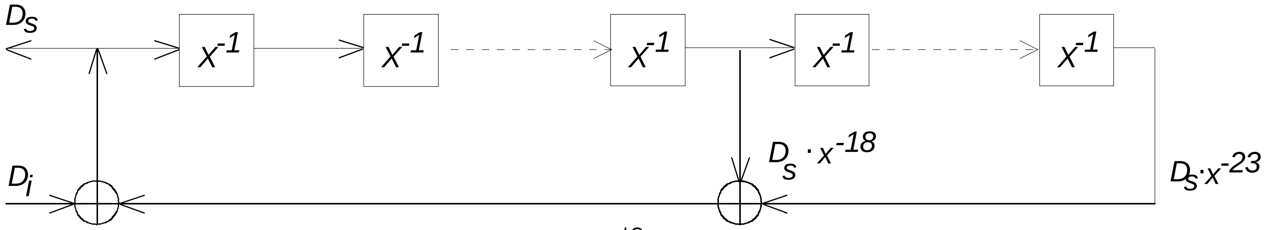
- $1 \oplus x^{-18} \oplus x^{-23}$

where $\oplus$ = modulo 2 summation.

The binary data stream shall be recovered in the receiver by applying the same polynomial to the scrambled data as was used in the transmitter.

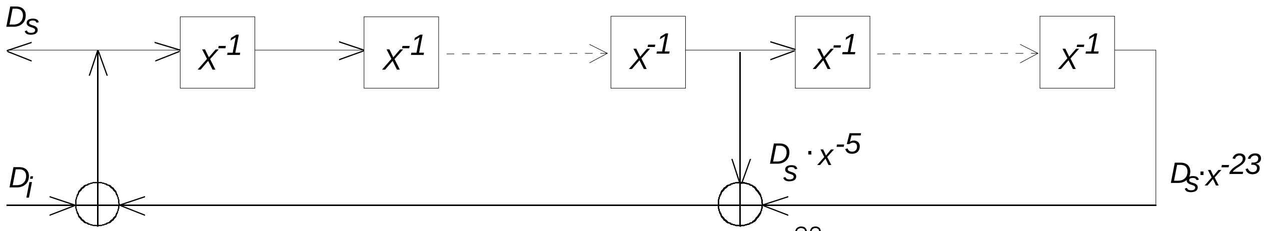
Binary ONEs and ZEROs entering the NT1 transceiver from the interface at reference point T or entering the LT side transceiver from the network shall appear as ONEs and ZEROs respectively, at the input of the scrambler. Also, during transmission/reception of the frame word or inverted frame word, the state of the scrambler shall remain unchanged. (Caution: It is common for the input bits to be all ONEs, e.g. during idle periods or during start-up. For the ONEs to become scrambled, the initial state of the scrambling shift register shall not be all ONEs).

NT1 transmit scrambler (NT1 to LT):



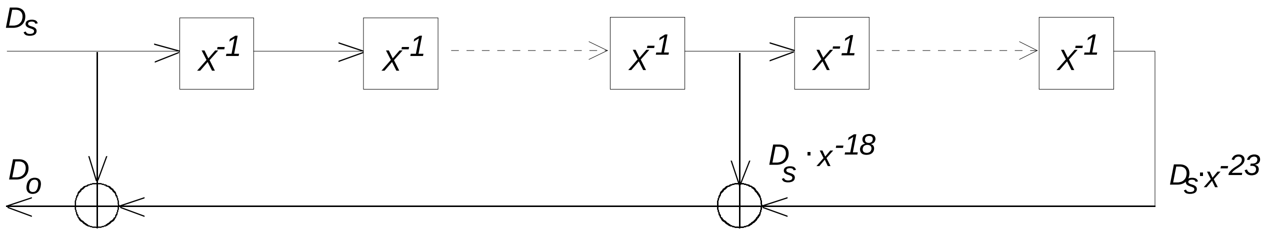
$$D_S = D_i \oplus D_S x^{-18} \oplus D_S x^{-23}$$

LT transmit scrambler (LT to NT1):



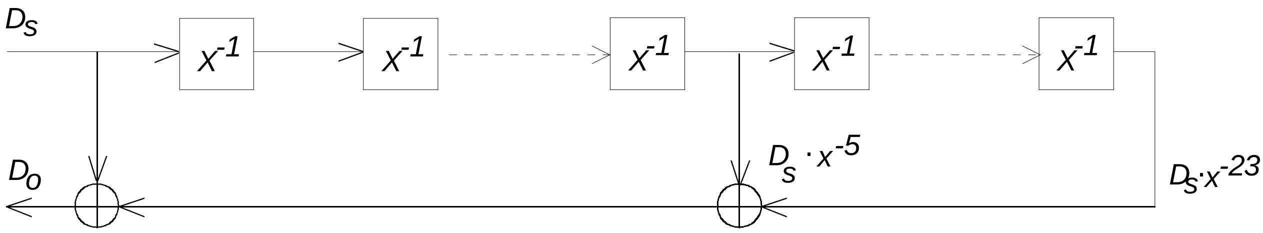
$$D_S = D_i \oplus D_S x^{-5} + D_S x^{-23}$$

LT receive descrambler (NT1 to LT):



$$D_O = D_S (1 + x^{-18} + x^{-23})$$

NT1 receive descrambler (LT to NT1):



$$D_O = D_S (1 + x^{-5} + x^{-23})$$

Figure A.5: Scrambler and descrambler

A.10 Start-up and control

This clause gives requirements for the start-up and turn-off processes, including examples of activation/deactivation requests, indicators of activation and deactivation and indicators of errors. The transmission system is capable of loopbacks. These are illustrated in tables A.3 and A.4. A specification of a procedure enabling the transmission system to be activated without activating the interface at reference point T is given in annex A1 on extension functions.

The following definitions are for the purpose of clarifying requirements which follow:

1) **Total Activation:** The word activation is used here to describe a process that includes the start-up process as given in (2) and activation as given in ETS 300 012 [1].

2) **Start-Up:** A process characterized by a sequence of signals produced by the LT and by the NT1. Start-up results in establishment of the master-slave mode, i.e. synchronization of the receivers and the training of equalizers and echo cancellers to the point that two-way transmission requirements are met.

3) **Warm-Start:** The start-up process that applies to transceivers meeting the optional warm-start activation-time requirements after they have once been synchronized and have subsequently responded to a deactivation request. Warm start applies only if there have been no changes in line characteristics and equipment. Transceivers that meet warm-start requirements are called warm-start transceivers.

4) **Cold-Start:** The start-up process that applies to transceivers that either do not meet optional warm-start activation-time requirements, or have not been continuously in a deactivated state that resulted from a deactivation request to the NT1. Cold-start also applies if there have been changes in line characteristics or equipment or both. A cold-start shall always start from the RESET state.

5) **Cold-Start-Only:** NT1 transceivers that do not meet optional warm-start activation-time requirements (see subclause A.10.6) are called cold-start-only transceivers. The use of cold-start-only transceivers is outside the scope of the present document.

6) **Full Operational Status:** Full operational status of a transceiver means that it has:

   a) acquired bit timing (for NT1), bit timing phase (for LT), and frame synchronization from the incoming signal from the other transceiver;

   b) recognized the incoming multiframe marker; and

   c) fully converged both echo canceller and equalizer coefficients.

7) **Deactivation:** The word deactivation is used here to describe a process that includes the turn-off process as given in 8) and deactivation of the S/T interface as given in ETS 300 012 [1].

8) **Turn-off:** The process by which a pair of fully operational transceivers transition to the RESET state.

9) **RESET:** The RESET state consists of two sub-states: the RECEIVE RESET and the FULL RESET states. In other clauses, the term RESET is used to refer to the FULL RESET state.

   RESET has no implications about the state of convergence of the equalizer or echo canceller coefficients of the transceiver.

   For specific transceiver implementations, RESET states (or sub-states) may mean different and possibly multiple internal states.

10) **FULL RESET:** The FULL RESET state is one in which a transceiver has detected the loss of signal from the far-end and is not transmitting (sending signal to the DLL).

   The FULL RESET state shall also be entered following power up.

   While in FULL RESET, NT1s may initiate transmission only if responding to a new power off/on cycle or to a new request for service from the customer Terminal Equipment (TE). Under all other conditions where the transceivers have been turned-off (see subclause A.10.1.5.2), the NT1s shall remain quiet, i.e. they shall not start transmitting any signal until they have received the TL signal (start-up tone) from the network.

11) **RECEIVE RESET:** The RECEIVE RESET state is a transient state in which NT1 has detected the loss of signal from the far-end and is not transmitting (sending signal to the DLL). In addition, the transceiver is not permitted to initiate the start-up sequence (send wake-up tone) but shall be capable of responding to the start-up sequence (detecting wake-up tone). Unless it responds to a wake-up tone, an NT1 must remain in this state for at least 40 ms, transceiver shall enter the FULL RESET state.

12) **Power Down Mode:** Power down is required to permit the digital transmission system to be placed in a low power consumption mode when no calls are in progress. The NT1 consumes less power but is capable of detecting TL from the network side and/or INFO1 from the user side.

13) **Transparency:** The word transparency is used to mean that the B_1-channel, B_2-channel, and D-channel (2B+D) bits received by the transceiver on the interface are passed to the TE at the NT and to the network at the LT. Likewise, when a transceiver is transparent, 2B+D bits sent to the transceiver at the LT from within the network, or at the NT from the TE, are transmitted on the interface. Conversely, when a transceiver is not transparent, 2B+D bits received on the interface are not passed along to the TE at the NT or to the network at the LT. Likewise, when a transceiver is not transparent, 2B+D bits from within the network at the LT or from the TE at the NT are not transmitted on the interface. Transparency applies separately to each transceiver. Conditions for transparency are discussed in subclause A.10.3.4.

A.10.1 Signals used for start-up and control

A.10.1.1 Signals during start-up

Figure A.6 defines the signals produced by the transceivers during start-up. These signals apply during both types of start-up; i.e. cold-start and warm-start. During start-up, all signals at the interface shall consist of sequences of symbols of the shape defined in subclause A.13.2.

With the exception of the wake-up tones (TN and TL), the scrambler shall be used in the normal way in formulating the signals. For example, figure A.7 shows ONEs for B and D channel bits and the overhead bits in the signal SN1. These ONEs are scrambled before coding, producing random pulses in these positions at the interface.

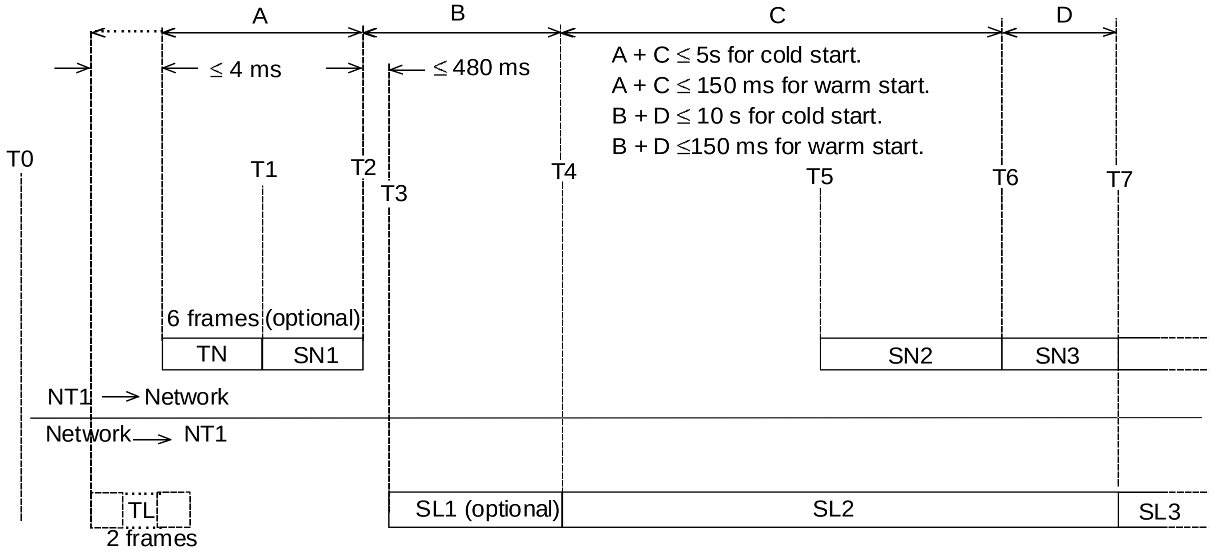
Except where noted otherwise in figure A.7, all the pulse sequences are framed and multiframed in accordance with the normal frame structure shown in figures A.1, A.2 and A.3 and all pulses represent scrambled bits except those in the frame word. The signals TN and TL are 10 kHz tones generated by repeating the following unscrambled and unframed symbol pattern:

... +3 +3 +3 +3 -3 -3 -3 -3...

A.10.1.2 Line rate during start-up

During start-up, the network shall produce symbols at the nominal line rate within the tolerance specified in subclause A.2.2.

The symbol rate from the NT shall be 80 kbaud ± 100 ppm.



Time: Description of event or state:

T0 RESET state.

T1 Network and NT1 are awake.

T2 NT1 discontinues transmission, indicating that the NT1 is ready to receive signal.

T3 Network responds to termination of signal and begins transmitting signal towards to NT1.

T4 Network begins transmitting SL2 towards the NT1, indicating that the network is ready to receive SN2.

T5 NT1 begins transmitting SN2 towards the network, indicating that NT1 has acquired FW frame and detected SL2.

T6 NT1 has acquired multiframe marker and is fully operational.

T7 Network has acquired multiframe marker and is fully operational.

NOTE 1: If the TL tone is repeated due to the persistence of FE 1, the repetition interval shall be > 25 ms. At a repetition interval larger than 480 ms, the state machine will cause a TL tone if FE 1 remains.

NOTE 2: The maximum time between TL tone and TN tone is defined to be 4 ms. This requirement is unnecessarily strict. To allow transceivers which cannot meet this the LT should wait for, and accept the TN tone, for a period of 10 ms from the beginning of issuing the TL tone.

Figure A.6: State sequence for transceiver start-up

A.10.1.3 Start-up sequence

Figure A.6 shows the sequence of signals at the interface that are generated by the transceivers. The transition points in the sequence are also defined in figure A.7. For further information on the events at the interface at reference point T, see ETS 300 012 [1].

A.10.1.4 Wake-up

When transceivers are in the RESET state or are deactivated, as a result of responding to a deactivation request, either transceiver may initiate start-up by sending a tone as defined in figure A.7.

A.10.1.5 Progress indicators

A.10.1.5.1 Start-up

In the NT1 to LT direction, the ACT bit remains set to ZERO until the customer equipment indicates progress in getting ready to transmit. The corresponding action at the T reference point in the customer equipment is receipt of the signal INFO3. To communicate this progress indication, ACT from the NT1 is set to ONE. Assuming INFO3 occurs before T6 and T7, this progress indication shall not affect overhead symbols at the interface until T6, when the NT1 overhead bits are allowed to be normal, and may not be detected by the LT until T7.

After event T7 (see figure A.6) and after ACT = ONE is received from the NT1, the LT sets the ACT bit to ONE to communicate readiness for layer 2 communication (see subclause A.8.3.2.2).

A.10.1.5.2 Deactivation

All transceivers shall cease transmission following loss of received signal. There are different turn-off procedures for transceivers that have achieved full operational status than for transceivers that have not (see subclause A.10.2).

The network may take advantage of the capabilities of warm-start NT1s by announcing turn-off. In announcing turn-off, the network shall change DEA from ONE to ZERO in at least three consecutive multiframes before ceasing transmission. It shall cease transmission before sending the DEA bit in the multiframe following the multiframe in which DEA = ZERO is sent for the last time.

During multiframes with DEA = ZERO, the NT1 has time to prepare for turn-off.

After the warm-start NT1 has prepared itself for turn-off, it shall upon detection of loss of signal from the network, cease transmission, and enter the RECEIVE RESET state within 40 ms of the occurrence of the transition to no signal at its interface. As specified in subclause A.10.2, unless it responds to a TL signal from the network, it shall not initiate the transmission of wake-up tone for a period of at least 40 ms after it ceases transmission, and then it shall enter the FULL RESET state.

The network side transceiver, after announcing turn-off and ceasing transmission, shall enter the FULL RESET state upon detection of loss of received signal from the NT1.

Although NT1s are not permitted to initiate turn-off, the LT shall respond to loss of signal as stated above.

A.10.2 Timers

Timers shall be used to determine entry into the RESET states. Upon the occurrence of any of the following conditions:

1) failure to complete start-up within 15 s (warm or cold start);

2) loss of received signal for more than 480 ms; or

3) loss of synchronization for more than 480 ms.

When a transceiver ceases transmission it shall enter the RECEIVE RESET state. It shall remain there at least 40 ms unless it responds to a wake-up tone. After this it shall enter the FULL RESET state if no wake-up tone was received. If a wake-up tone was received it may immediately respond with a TN-tone. The manner of entering the RECEIVE RESET state is different for the different conditions listed above.

The transceiver, when entering either in loss of signal state or loss of synchronization, shall not enter into the RESET state as long as a timer of 480 ms has not elapsed.

For conditions 1) or 3), it shall cease transmission and then, upon the subsequent detection of the loss of received signal, the transceiver shall enter the RECEIVE RESET state. Its response time to a loss of signal (after conditions 1) or 3) have been satisfied) shall be such that it shall enter the RECEIVE RESET state and be capable of responding to the initiation of wake-up tone by the far-end transceiver within 40 ms after the far end transceiver ceases transmission.

For condition 2), the transceiver shall immediately enter the RECEIVE RESET state.

For conditions 2) and 3), these requirements apply to transceivers after multiframe synchronization is achieved (see T6 and T7 in figure A.6).

In addition, an NT1 shall enter the FULL RESET state if signal is not received within 480 ms after it ceases the transmission of TN, or SN1 if it is sent (see T2 to T3 in figures A.6 and A.7).

A.10.3 Description of the start-up procedure

A.10.3.1 Start-up from customer equipment

While the NT1 and LT remain in the deactivated state as a result of receiving and responding to a deactivation request, or while they are in RESET, a request for activation from the customer equipment shall result in the TN signal (tone) being sent from the NT1 towards the LT. The LT, on receiving TN shall remain silent until detection of cessation of signal from the NT1. The rest of the sequence then follows as indicated in figures A.6 and A.7. If the LT happens to try to activate at the same time it may send a TL tone during the TN tone without harm.

For cold-start-only NT1s, start-up shall be attempted upon NT1 power-up. After an unsuccessful start-up attempt, the NT1 DLL transceiver may enter FULL RESET.

While in the RESET state, NT1s may initiate transmission only if responding to a new power off/on cycle or a new service request. Under all other conditions where the system has been deactivated, the NT1s shall remain quiet, i.e. they shall not start transmitting any signal until the NT1 has received the TL signal from the LT.

A.10.3.2 Start-up from the network

While the NT1 and LT remain in the deactivated state as a result of receiving and responding to a deactivation request, or while they are in RESET, a request for activation from the LT shall result in the TL signal being sent from the LT towards the NT1. The NT1, on receiving TL shall respond with TN within 4 ms from the beginning of TL. The rest of the sequence then follows as indicated in figures A.6 and A.7.

A.10.3.3 Sequence charts

Examples of sequence charts for start-up by both terminal and ET equipment are given in figures A.8 and A.9.

Signal	Frame Word (FW)	Multi-frame (IFW)	2B+D	M	Start	Stop	Time (Frames)
TN	±3 ‡	±3 ‡	±3 ‡	±3 ‡	†	†	6
SN1	Present	Absent	1	1	T1	T2	-
SN2	Present	Absent	1	1	T5	T6	-
SN3	Present	Present	Normal^{+}	Normal	T6	*	-
TL	±3 ‡	±3 ‡	±3 ‡	±3 ‡	†	†	2
SL1	Present	Absent	1	1	T3	T4	-
SL2	Present	Present	0	Normal	T4	T7	-
SL3	Present	Present	Normal^{+}	Normal	T7	*	-

Symbols and abbreviations:

‡ Tones have alternating pattern of four +3 symbols followed by four -3 symbols and no FW.

† See figure A.6 and subclause A.10.1.3 for start and/or stop time of this signal.

TN,TL Tones produced by NT1 or LT, respectively (see subclause A.10.1.1).

SNx, SLx Pulse patterns produced by NT1 or LT, respectively.

Tx Notation refers to transition instants defined in figure A.6.

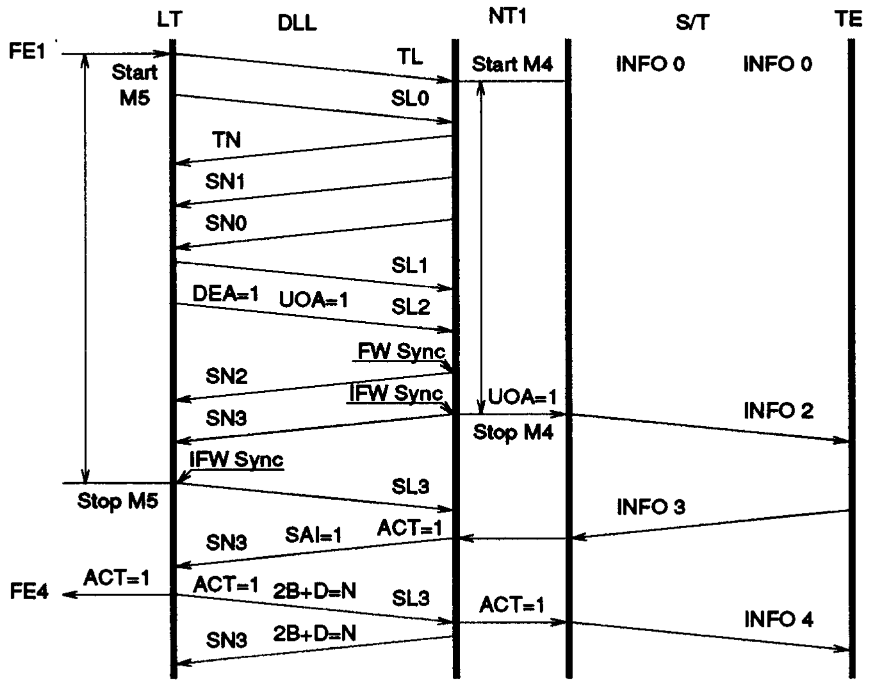
Absent Under multiframe, this notation means only that FW is transmitted instead of IFW.

Normal Normal means that the M bits are transmitted onto the 2-wire line as required during normal operation; e.g. valid CRC bits, EOC bits and indicator bits are transmitted.

Normal^{+} Except to perform a loopback, 2B+D bits shall remain in the previous state (SN2 or SL2) until both ACT bits indicate full transparency of the B and D channels (i.e. the 2B+D bits of SN3 and SL3 shall remain set to ONE and ZERO, respectively, until transparency is achieved at both ends of the DLL).

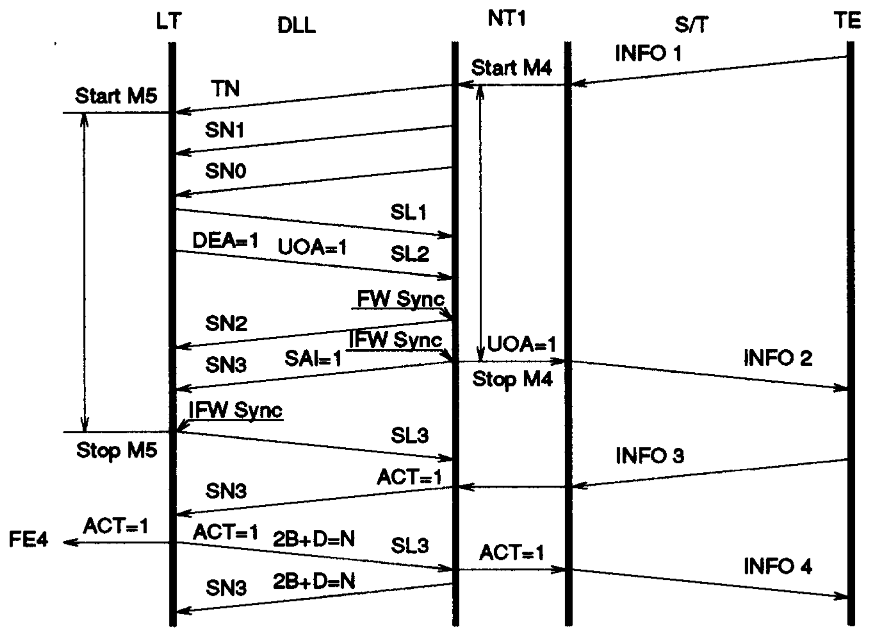
* Signals SN3 and SL3 continue indefinitely (or until turn-off).

Figure A.7: Definitions of signals during start-up



NOTE 1: Receipt of INFO3 and SL3 at the NT1 can theoretically occur in either order.
NOTE 2: For symbols and abbreviations see table A.5.
NOTE 3: The reading of the UOA bit is necessary only when the option "DLL-only turn-on" is implemented.

Figure A.8: Total activation initiated by the exchange



NOTE 1: Receipt of INFO3 and SL3 at the NT1 can theoretically occur in either order.
NOTE 2: For symbols and abbreviations see table A.5.
NOTE 3: The reading of the UOA bit is necessary only when the option "DLL-only turn-on" is implemented.

Figure A.9: Total activation initiated by terminal equipment

A.10.3.4 Transparency

Transparency of the transmission in both directions by the NT1 shall be provided after the NT1 achieves full operational status (T6), and both ACT = ONE from the LT and DEA = ONE. Full operational status of the NT1 means that the NT1 has:

1) acquired bit timing and frame synchronization from the incoming signal from the LT;

2) recognized the multiframe marker from the LT; and

3) fully converged both its echo canceller and equalizer coefficients.

Transparency of the transmission in both directions at the LT shall be provided when the LT:

1) achieves full operational status (T7);

2) detects the presence of the multiframe marker from the NT1; and

3) receives ACT = ONE from the NT1.

Full operational status at the LT means that the LT has:

1) acquired bit timing phase of the incoming signal from the NT1 and frame synchronization;

2) recognized the multiframe marker from the NT1; and

3) fully converged both its echo canceller and equalizer coefficients.

At the LT, transparency of the B-channels and D-channel shall occur at any time during either the first LT transmitted super frame with ACT = ZERO or during the last LT transmitted super frame with ACT = ZERO. Transparency occurs at the transition from all ZEROs to "Normal" in the B-channels and D - channel in SL3. For example, referring to figure A.1, suppose super frame A is the last transmit super frame with ACT = ZERO, super frame B is the first transmit super frame with ACT = ONE, and super frames C and D continue with ACT = ONE. The transition to transparency may occur not later than the first bit of super frame C. This means that all B-channel and D-channel bits in super frames C and D shall be transmitted transparently, provided that conditions for transparency have been maintained.

At the LT, transparency of the B-channels and D-channels in the LT to network direction may occur at a different time than transparency in the LT to NT direction. However, in both directions the LT shall become transparent during the two transmit super frames A and B described in the example. The NT may not yet have achieved transparency during this interval.

After both the LT and the NT1 achieve transparency in both directions, the ACT bits shall continue to reflect the state of readiness of the LT and the terminal equipment for layer 2 communication. The ACT bit in the LT to NT1 direction shall reflect the status of the LT side of the interface. The ACT bit in the NT1 to LT direction shall reflect the status of the NT1 side of the interface. Whenever either end, for any reason, loses its readiness to communicate at layer 2 (e.g. the terminal is unplugged), that end shall set its transmitted ACT bit to ZERO. A change of status of this bit shall be repeated in at least three consecutive transmitted multiframes.

A.10.4 State transition table for the NT1

Table A.3 provides an example of a state transition table for the NT1 as a function of INFOs, SIGs, and timers.

A.10.5 State transition table for the LT

Table A.4 provides an example of a state transition table for the LT as a function of FEs, SIGs, and timers.

Table A.3: State transition table for the NT1 as a function of INFOs, SIGs and timers - with loopback 2: an example

	State name	**Power off**	**Full reset**	**Alerting**	**EC Training (optional)**	**EC converged**	**FW sync**	**IFW sync**	**Pending active**	**Active**	**Pending deacti-vation**	**Tear down**	**Receive reset**	**Loopback 2 initiated**	**Loopback 2 pending**	**Loopback 2 operated**
	State code (figure A.6 event)	**NT0**	**NT1 (T0)**	**NT2**	**NT3 (T1)**	**NT4 (T2)**	**NT5 (T5)**	**NT6 (T6)**	**NT7**	**NT8**	**NT9**	**NT10**	**NT12**	**NT6A**	**NT7A**	**NT8A**
Event ↓	**Signal → LT** **Signal → TE (note 2)**	**SN0** **INFO 0**	**SN0** **INFO 0**	**TN** **INFO 0**	**SN1** **INFO 0**	**SN0** **INFO 0**	**SN2** **INFO 0**	**SN3 ACT=0** **INFO 2**	**SN3 ACT=1** **INFO 2**	**SN3 ACT=1** **INFO 4**	**SN3 (note 8)**	**SN0** **INFO 0**	**SN0** **INFO 0**	**SN3 ACT=0** **INFO 2 (note 17)**	**SN3 ACT=1** **INFO 2 (note 17)**	**SN3 ACT=1** **INFO 4 (note 17)**
Power ON		NT1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Loss of power		-	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0
Received new INFO 1 (note 2)		/	ST.M4 NT2 (note 12)	-	-	-	-	-	/	/	-	-	-	/	/	/
Receive INFO 3 (SL2 or SL3) (ACT=0, DEA=1) (note 2)		/	/	/	/	/	/	NT7	-	-	-	-	-	NT7A (note 17)	-	-
INFO 0 (LOS/LFA at T) (SL2 or SL3) (note 2)		/	-	-	-	-	-	-	NT6	NT6	-	-	-	-	NT6A (note 17)	NT6A (note 17)
End of tone TN (9 ms)		/	/	NT3 or NT4	/	/	/	/	/	/	/	/	/	/	/	/
Received tone TL		/	ST.M4 NT2	-	/	/	/	/	/	/	/	/	ST.M4 STP.M6 NT2	/	/	/
Echo canceller converged		/	-	-	NT4	-	-	-	-	-	-	-	-	-	-	-
FW sync and detect SL2		/	/	/	/	NT5	-	-	-	-	-	-	/	-	-	-
IFW sync (SL2)		/	/	/	/	/	STP.M4 NT6	-	-	-	-	-	/	-	-	-
Received DEA=0 (SL2 or SL3) (note 6)		/	/	/	/	/	/	NT9	NT9	NT9	-	-	/	NT9	NT9	NT9
Received (SL2 or SL3) ACT=0 and DEA=1		/	/	/	/	/	/	-	-	NT7	NT6,NT6A NT7,NT7A (note 13)	-	/	-	-	NT7A

	State name	Power off	Full reset	Alerting	EC Training (optional)	EC converged	FW sync	IFW sync	Pending active	Active	Pending deacti-vation	Tear down	Receive reset	Loopback 2 initiated	Loopback 2 pending	Loopback 2 operated
	State code (figure A.6 event)	**NT0**	**NT1 (T0)**	**NT2**	**NT3 (T1)**	**NT4 (T2)**	**NT5 (T5)**	**NT6 (T6)**	**NT7**	**NT8**	**NT9**	**NT10**	**NT12**	**NT6A**	**NT7A**	**NT8A**
	Signal → LT	**SN0**	**SN0**	**TN**	**SN1**	**SN0**	**SN2**	**SN3 ACT=0**	**SN3 ACT=1**	**SN3 ACT=1**	**SN3 (note 8)**	**SN0**	**SN0**	**SN3 ACT=0**	**SN3 ACT=1**	**SN3 ACT=1**
Event ↓	**Signal → TE (note 2)**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 2**	**INFO 2**	**INFO 4**		**INFO 0**	**INFO 0**	**INFO 2 (note 17)**	**INFO 2 (note 17)**	**INFO 4 (note 17)**
Received (SL3) ACT=1and DEA=1		/	/	/	/	/	/	-	NT8	-	NT8, NT8A (note 13)	-	/	-	NT8A	-
Loss of synchronization (> 480 ms)		/	/	/	/	/	/	NT10	NT10	NT10	NT10	-	-	NT10	NT10	NT10
Loss or absence of signal (> 480 ms) (note 14)		/	/	/	/	STP.M4 NT1	-	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	/	/	-	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12
Expiry of timer M4 (15 seconds)		/	/	/	NT10	NT10	NT10	/	/	/	/	/	-	/	/	/
Loss of signal < 40 ms		/	/	/	/	-	-	-	-	-	ST.M6 NT12	ST.M6 NT12	/	-	-	-
Expiry of timer M6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	NT1	/	/	/
Received EOC (SL3) "Loopback 2" request (note 18)		/	/	/	/	/	/	NT6A	NT6A	NT6A	/	/	/	-	-	-
Received EOC "Return to Normal" Request		/	/	/	/	/	/	-	-	-	-	-	/	NT6 (note 19)	NT6 (note 19)	NT6 (note 19)

NOTE: For symbols, abbreviations and notes, see table A.5.

Table A.4: State transition table for the LT as a function of FEs, SIGs and timers - with loopback 2: an example

Event ↓ / State name	Power off	Full reset	Alerting	Awake	EC Training (optional)	EC converged	FW sync	IFW sync	Active	Deacti-vation alerting	Tear down	Pending deacti-vation	Receive reset	Loopback 2 requested	Loopback 2 operated
State code (figure A.6 event)	**LT0**	**LT1 (T0)**	**LT2**	**LT3 (T1)**	**LT4 (T3)**	**LT5 (T4)**	**LT6**	**LT7 (T7)**	**LT8**	**LT9**	**LT10**	**LT11**	**LT12**	**LT7A**	**LT8A**
Signal → NT	**SL0**	**SL0**	**TL**	**SL0**	**SL1**	**SL2 DEA=1 ACT=0**	**SL2 DEA=1 ACT=0**	**SL3 DEA=1 ACT=0**	**SL3 DEA=1 ACT=1**	**SL3 DEA=0 ACT=0**	**SL0**	**SL0**	**SL0**	**SL3 DEA=1 ACT=0 (note 17)**	**SL3 DEA=1 ACT=1 (note 17)**
Power ON	LT1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Loss of power (note 1)	-	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7
Activation request (FE1) or "Loopback 2 Request" (FE8) (note 1)	-	ST.M5 LT2 FE2	-	-	-	-	-	-	-	-	-	-	-	-	-
Deactivation request (FE5) (notes 1 and 9)	-	-	-	-	-	-	-	LT9	LT9	-	-	-	-	LT9	LT9
End of tone TL (3 ms) Continue FE1 or FE8 (note 1)	/	/	LT3	/	/	/	/	/	/	/	/	/	/	/	/
Received tone TN Continue FE1 or FE8 (note 1)	/	ST.M5 LT3 FE2	-	-	/	/	/	/	/	/	/	/	ST.M5 STP.M7 LT3 FE2	/	/
Loss of signal energy (TN or SN1) Continue FE1 or FE8 (note 1)	/	/	-	LT4 or LT5	-	/	/	/	/	/	/	/	/	/	/
Echo canceller converged Continue FE1 or FE8 (note 1)	/	-	-	-	LT5	-	-	-	-	-	-	-	-	-	-
FW sync (SN2 or SN3) Continue FE1 or FE8 (note 1)	/	/	/	/	/	LT6	-	-	-	-	-	-	/	-	-
IFW sync (SN3) Continue FE1 or FE8 (note 1)	/	/	/	/	/	/	STP.M5 LT7 FE3	-	-	-	-	-	/	-	-
Received ACT=0 (SN3) (note 1)	/	/	/	/	/	/	/	-	LT7 FE12	-	-	-	/	-	LT7A FE12

	State name	Power off	Full reset	Alerting	Awake	EC Training (optional)	EC converged	FW sync	IFW sync	Active	Deacti-vation alerting	Tear down	Pending deacti-vation	Receive reset	Loopback 2 requested	Loopback 2 operated
	State code (figure A.6 event)	**LT0**	**LT1 (T0)**	**LT2**	**LT3 (T1)**	**LT4 (T3)**	**LT5 (T4)**	**LT6**	**LT7 (T7)**	**LT8**	**LT9**	**LT10**	**LT11**	**LT12**	**LT7A**	**LT8A**
Event ↓	**Signal → NT**	**SL0**	**SL0**	**TL**	**SL0**	**SL1**	**SL2 DEA=1 ACT=0**	**SL2 DEA=1 ACT=0**	**SL3 DEA=1 ACT=0**	**SL3 DEA=1 ACT=1**	**SL3 DEA=0 ACT=0**	**SL0**	**SL0**	**SL0**	**SL3 DEA=1 ACT=0 (note 17)**	**SL3 DEA=1 ACT=1 (note 17)**
Received ACT=1 (SL3) (FE1) (note 1)		/	/	/	/	/	/	/	LT8 FE4	-	-	-	-	/	LT8A FE4	-
Loss of synchronization (> 480 ms) (note 1)		/	/	/	/	/	/	/	LT10 FE7	LT10 FE7	LT10 FE7	-	-	-	LT10 FE7	LT10 FE7
Loss or absence of signal (> 480 ms) (note 1)		/	/	/	LT1	/	-	-	ST.M7 LT12 FE7	ST.M7 LT12 FE7	ST.M7 LT12 FE7	-	-	-	ST.M7 LT12 FE7	ST.M7 LT12 FE7
End of last super frame with DEA=0 (FE5) (note 10)		/	/	/	/	/	/	/	/	/	LT11	/	/	/	-	/
Expiry of timer M5 (15 seconds) (note 1)		/	/	/	LT10 FE7	LT10 FE7	LT10 FE7	LT10 FE7	/	/	/	/	/	/	/	/
Absence of signal < 40 ms (note 1)		/	-	/	/	/	-	-	-	-	-	ST.M7 LT12	LT1 FE6	-	-	-
Expiry of timer M7 (40 ms) (note 1)		/	/	/	/	/	/	/	/	/	/	/	/	LT1 FE6	/	/
Loopback 2 Request (FE8) (notes 1 and 18)		/	/	/	/	/	/	/	LT7A	LT7A	-	-	-	-	-	-
Return to Normal Request		/	/	/	/	/	/	/	-	-	-	-	-	-	(note 19) LT7 FE12	(note 19) LT7 FE12

NOTE: For symbols, abbreviations and notes, see table A.5.

Table A.5: Symbols, abbreviations and notes for tables A.3 and A.4

Symbols, abbreviations and notes for tables A.3 and A.4		
Symbols and abbreviations		
"-"	=	No change, no action.
"/"	=	Impossible or prohibited situation under normal circumstances.
"FE1"	=	Activate Access Request (AR) (note 1).
"FE2"	=	Access Activation Initiated (note 1).
"FE3"	=	Line Transceivers Activated (note 1).
"FE4"	=	Access Activated or Loopback Operated (AI) (note 1).
"FE5"	=	Deactivate Access Request (note 1).
"FE6"	=	Access or Loopback Deactivated (DI) (note 1).
"FE7"	=	LOS/LFA in Line Transceivers - (including Loss of Power at NT1) (note 1).
"FE8"	=	Activate Loopback 2 (note 1).
"FE9"	=	Activate Loopback 1 (at LT towards network) (note 1).
"FE10"	=	Activate Loopback 1a (at Regenerator towards network) (note 1).
"FE11"	=	Partial Activation Request (UOA) (see subclause A.8.3.2.7) (note 1).
"FE12"	=	Report LOS/LFA at T reference point (see subclause A.8.3.2.8).
"FE13"	=	Deactivate the interface at T reference point whilst keeping the Access Digital Section activated (note 1).
"NTn"	=	Go to state "NTn".
"LTn"	=	Go to state "LTn".
"ST.Mn"	=	Start timer Mn.
"STP.Mn"	=	Stop timer Mn.
"SLn,SNn"	=	Signals defined in figures A.6 and A.7 (SL0, SN0 = no signal) SN0 and SL0 are silent signals which shall have a level of less than -45 dBm, when measured between 5 kHz and 50 kHz.
"Tn"	=	Events defined in figures A.6 and A.7.

NOTES:

NOTE 1: The function elements are also defined in subclause 8.4.3 of ETS 300 297 [4].
NOTE 2: INFO signals at the T reference point are defined in subclause A.6.2.2 of ETS 300 012 [1].
NOTE 3: Void.
NOTE 4: Void.
NOTE 5: Void.
NOTE 6: Cold-start-only NTs may ignore this event.
NOTE 7: Void.
NOTE 8: The signals output in this state remain unchanged from signals output during the preceding state (for example, ACT=0 if state NT6 preceded, or ACT=1 if states NT7 or NT8 preceded). The INFOs also remain unchanged.
NOTE 9: This event is only the first step of a sequence leading to deactivation. After transmitting DEA=0 for a short interval (see note 10), the LT sends SL0 to deactivate the NT.
NOTE 10: This event occurs as a result of FE5 (see note 9) after entering state LT9 and transmitting at least three super frames with DEA=0 (see subclause A.10.1.5).
NOTE 11: Void.
NOTE 12: When INFO 1 remains continuous after the NT fails to bring up the network side and returns to state NT1, the NT does not go again into state NT2 unless a new transition from INFO 0 to INFO 1 is received (see clause A.10 (10) and ETS 300 012 [1]).
NOTE 13: The transceiver should return to the state from which it entered state NT9, unless the UOA or ACT bit(s) have changed.
NOTE 14: The transitions resulting from this event, to either full reset (NT1) or receive reset (NT12), are controlled by the requirements in subclause A.10.2.
NOTE 15: The network is permitted to choose "No action" rather than sending FE1 and transferring to state LT7. For example, when the access link is undergoing maintenance, "No action" is an appropriate response.
NOTE 16: Void.

Symbols, abbreviations and notes for tables A.3 and A.4
NOTE 17: When activation is for the purpose of performing a loopback (typical means of performing loopbacks for warm-start transceivers), FE8 initiates the activation at the LT and causes the LT to send the EOC loopback command, when the LT enters state LT7. The NT has achieved synchronization (NT6), and is sending INFO 2. If enough time elapses before confirmation of the EOC loopback command, the NT may enter state NT7 and send ACT=1 towards the LT as the TE responds with INFO 3. Furthermore, if the LT responds with ACT=1, the NT would enter NT8. It is preferable that the NT not enter NT8 in the process of responding to a loopback request (FE8). The network side should control the ACT bit sent by the LT so that it will not be sent in response to receipt of ACT=1 from the NT when the EOC loopback 2 command is being sent, or is about to be sent. This will keep the NT from entering NT8. Once the command is completed (including confirmation of correct receipt as described in subclause A.8.3.3.2), the LT should respond to ACT1 from the NT in the usual way. However, when cold-start-only LTs and NTs are used, the NT may be in NT8 prior to the decision to operate loopback 2. The NT will operate the loopback if the EOC command is received during state NT8. It is not necessary to turn off the transceivers (enter RESET) prior to issuing a loopback 2 command; for cold-start-only transceivers it would be normal to allow the transceivers to remain active. But, as with warm-start transceivers, it is preferable to force ACT=0 towards the NT prior to issuing the loopback command and to release the LT to respond to ACT=1 from the NT only when the EOC command has been completed and confirmed. When the loopback 2 command is received in states NT6, NT7 or NT8, the NT makes a transition to state NT6A. When entering NT6A from NT7 or NT8, the NT reverts to sending ACT=0 towards the LT. Furthermore, when the loopback 2 command is received in state NT8, the NT reverts to sending INFO 2 towards the TE. Also, during states NT6A, NT7A and NT8A, all INFO signals from the TE are blocked (prevented from reaching the T receiver in the NT). In state NT6A, the event "Receive INFO 3" is taken to mean that the T receiver in the NT is synchronized (or re-synchronized) with the T transmitter in the NT. At this point, the NT enters state NT7A and sends ACT=1 towards the LT. When the LT responds with ACT=1, the NT enters state NT8A and sends INFO 4 frames towards the TE containing D-channel and B-channel bits received from the LT and with the D-echo-channel bits set to ZERO (0). On entering NT7A, and in NT8A, the NT also replaces the ONEs (1s) data in the D-channel and B-channel towards the LT (normal+ in SN3) with data contained in the INFO signal towards the TE. Transparency of the NT in the NT to LT direction to data contained in the INFO signal towards the TE is co-ordinated with sending ACT=1 following rules given in clause A.10 (13) and subclause A.10.3.4. The B-channel and D-channel data from the LT towards the NT will initially be ZEROs (0s) (normal+ in SL3) until the LT becomes transparent. When the B-channel and D-channel data in the INFO signal from the NT towards the TE is used by the NT in its signal towards the LT, it will not contain the data sent by the LT until state NT8A is entered. This occurs from when the INFO signal is INFO 2 until the NT enters state NT8A. In state NT8A, both the LT and NT are transparent, the data sent from the LT is looped back towards the NT, and the loopback is also transparent, meaning that the data sent from the LT is also contained in INFO 4 towards the TE. In states NT7A and NT8A, the event "INFO 0 (LOS/LFA at T)" is taken to mean absence of synchronization or signal at the T receiver of the NT (the signal is either INFO 2 or INFO 4 from its own transmitter). In this case, the NT enters state NT6A (INFO 2 towards the TE and ACT=0 towards the LT). The D-channel and B-channel bits are not looped back in this case; the signal becomes all 1s in the D-channel and B-channel (normal+ in SL3).
NOTE 18: The EOC request is not sent before T7 (when the LT has achieved IFW sync). The NT has already sent SN3 before the LT can reach T7. Therefore, the LT is in state LT7 or higher and the NT is in state NT6 or higher before EOC commands are sent. (Theoretically, normal overhead bits, including EOC commands, may be sent in SL2 during state LT5, but the LT cannot receive the echoes required in the EOC protocol, described in subclause A.8.3.3.2, until T7).
NOTE 19: When the loopback has been released, the LT transitions from LT8A to LT7 where, as shown in table 2, a number of additional transitions are available. For warm-start transceivers, the "Return-to-Normal" request is usually the result of a deactivation request (FE5), and in that case, the LT transitions to state LT9 and sends DEA=0. After sending DEA=0 for at least three super frames, the LT transitions to LT11 in which SL0 is sent to the NT, FE6 is sent to the ET, and the access is deactivated. In this example, the NT is initially synchronized in state NT6, where it responds to receipt of DEA=0 by entering state NT9. Even when the presence of INFO 3 from the TE causes transition to NT7, before receipt of DEA=0, the end result is the same. Because the LT is in state LT9, it does not respond with ACT=1 if the NT sends ACT=1 (NT in state NT7), and the NT does not enter NT8. The NT then deactivates on recognition of loss of signal (SL0) from the LT. When EOC "Return to Normal" is sent without a deactivation request (FE5), (a process typically used for cold-start-only transceivers and not considered an option in these requirements) the transceivers remain synchronized in LT7 and NT6, respectively. Transparency depends on readiness for layer 2 communication at both ends and the consequent setting of ACT bits in both directions. For example, if the TE layer is already sending INFO 3 or responds with INFO 3, the NT then makes a transition to NT7. The LT will move from LT8A to LT7 (as shown) and then to LT8, where it sends ACT=1 when ACT=1 is received. After that, the NT moves to NT8 on receipt of ACT=1.

A.10.6 Activation times

The LT and the NT1 shall complete the start-up process, including synchronization and training of equalizers to the point of meeting performance criteria within the following lengths of time:

- the digital transmission system shall start up within 300 ms without REG and 600 ms with REG on warm-starts and within 15 s on cold-starts (with and without REG);
- without REG, the 15 s cold-start time requirement is apportioned such that the NT1 is allowed 5 s and the LT is allowed 10 s;
- with REG, the apportionment for NT1, REG and LT is for further study;
- for warm-starts the 300 ms start-up time requirement is apportioned equally between the NT1 and the LT, 150 ms each.

See figure A.6 for details.

NOTE 1: The 300 ms requirement applies to laboratory tests only. No 300 ms timer is involved in actual in-service DLLs (see definitions in clause A.10 for warm and cold-starts).

As indicated in figure A.6, the start time requirements cover the time span from wake-up tone to T7, and do not include time for activation of customer terminal equipment. All activation times apply only to the DLL, and do not apply to the entire customer access link where carrier systems may be involved.

NOTE 2: See subclause 8.5 in ETS 300 297 [4].

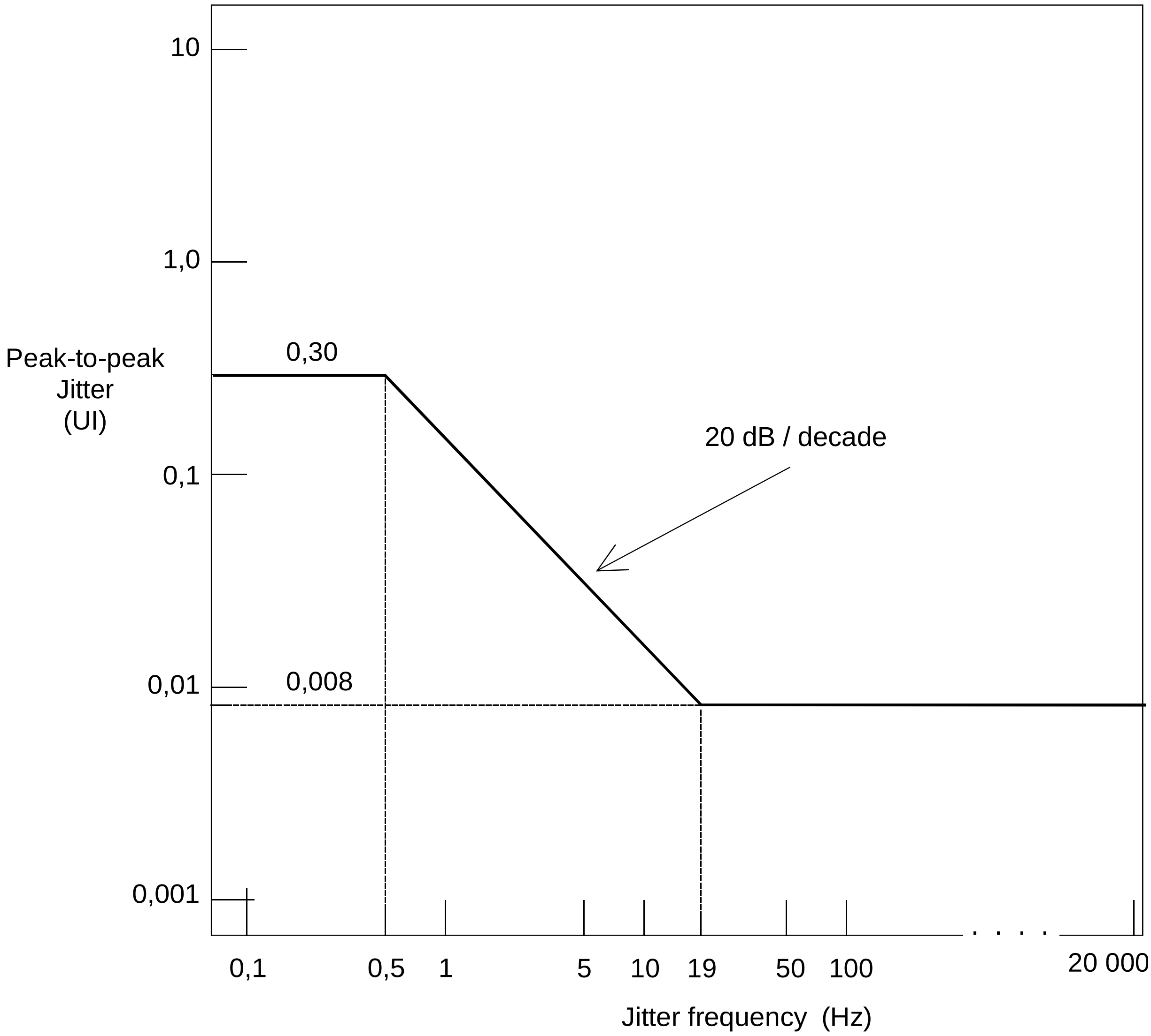
A.11 Jitter

Jitter tolerances are intended to ensure that the limits of ETS 300 012 [1] are supported by the jitter limits of the transmission system on local lines. The jitter limits given in this clause shall be satisfied regardless of the length of the local line and the inclusion of one regenerator, provided that they are covered by the transmission media characteristics (see clause 5). The limits shall be met regardless of the bit patterns in the B, D and C_L channels.

Jitter is specified in terms of Unit Intervals (UI) of the nominal 80 kbaud signal (12,5 μs).

A.11.1 NT1 input signal jitter tolerance

The NT1 shall meet the performance objectives with wander/jitter at the maximum magnitude indicated in figure A.10, for single jitter frequencies in the range of 0,1 Hz to 20 kHz on the LT output signal with the received signal baud rate in the range of 80 kbaud ± 5 ppm.



NOTE: Unit Interval (UI) = 12,5 µs.

Figure A.10: Permissible sinusoidal NT1 input signal jitter

A.11.2 NT1 output jitter limitations

With the wander/jitter as specified in subclause A.11.1, superimposed on the NT1 input signal, the jitter on the transmitted signal of the NT1 towards the LT shall conform to the following, with the received signal baud rate in the range of 80 kbaud ± 5 ppm as described in subclause A.2.1.2:

1) the jitter shall be equal to or less than 0,04 UI peak-to-peak and less than 0,01 UI rms when measured with a high-pass filter having a 6 dB per octave roll-off below 80 Hz;

2) the jitter in the phase of the output signal (the signal transmitted towards the LT) relative to the phase of the input signal (from the LT) shall not exceed 0,05 UI peak-to-peak and 0,015 UI rms when measured with a band-pass filter having a 6 dB per octave roll-off above 40 Hz and below 1,0 Hz (note that the 1,0 Hz cut-off assures that the average difference in the phase of the input and output signals is subtracted). This requirement applies with superimposed jitter in the phase of the input signal as specified in subclause A.11.1 for single frequencies up to 19 Hz;

3) the maximum (peak) departure of the phase of the output signal from its nominal difference (long term average) from the phase of the input signal (from the LT) shall not exceed 0,1 UI. This requirement applies during normal operation including following a "warm-start".

NOTE: This means that, if deactivated and subsequently activated in conformance with the "warm start" requirements, the long term average difference in phase of the output signal from the phase of the input signal is calculated over the whole activated time, even if several deactivations are in between.

A change of the input-output phase difference during an deactivation may not lead to stronger requirements of the LT-synchronization than given in section 1) and 2) of this subclause.

A.11.3 LT input signal jitter tolerance

The LT shall operate satisfactorily with input signal jitter equal to the worst case NT1 output signal jitter allowed by the limits set in subclause A.11.2.

A.11.4 LT output jitter and synchronization

The output signals from the LT shall not exceed the NT1 input signal jitter tolerance limits stated in subclause A.11.1. This requirements shall be met while maintaining data synchronization with the network.

A.11.5 REG jitter tolerance and output jitter limitations

The REG shall meet the performance objectives with wander/jitter received at its side directed towards the LT as stated in subclause A.11.1. The output signals from the REG shall not exceed the NT1 input signal jitter tolerance limits stated in subclause A.11.1. This requirement shall be met while maintaining data synchronization with the network.

A.11.6 Test conditions for jitter measurements

Due to bidirectional transmission on the 2-wire line and due to severe intersymbol interference, no well-defined signal transitions are available at the NT1 2-wire point.

Two possible solutions are proposed:

1) a test point in the NT1 is provided to measure jitter with an undisturbed signal;

2) a standard LT transceiver including an artificial transmission line is defined as a test instrument.

A.12 Transmitter output characteristics of NT1, REG and LT

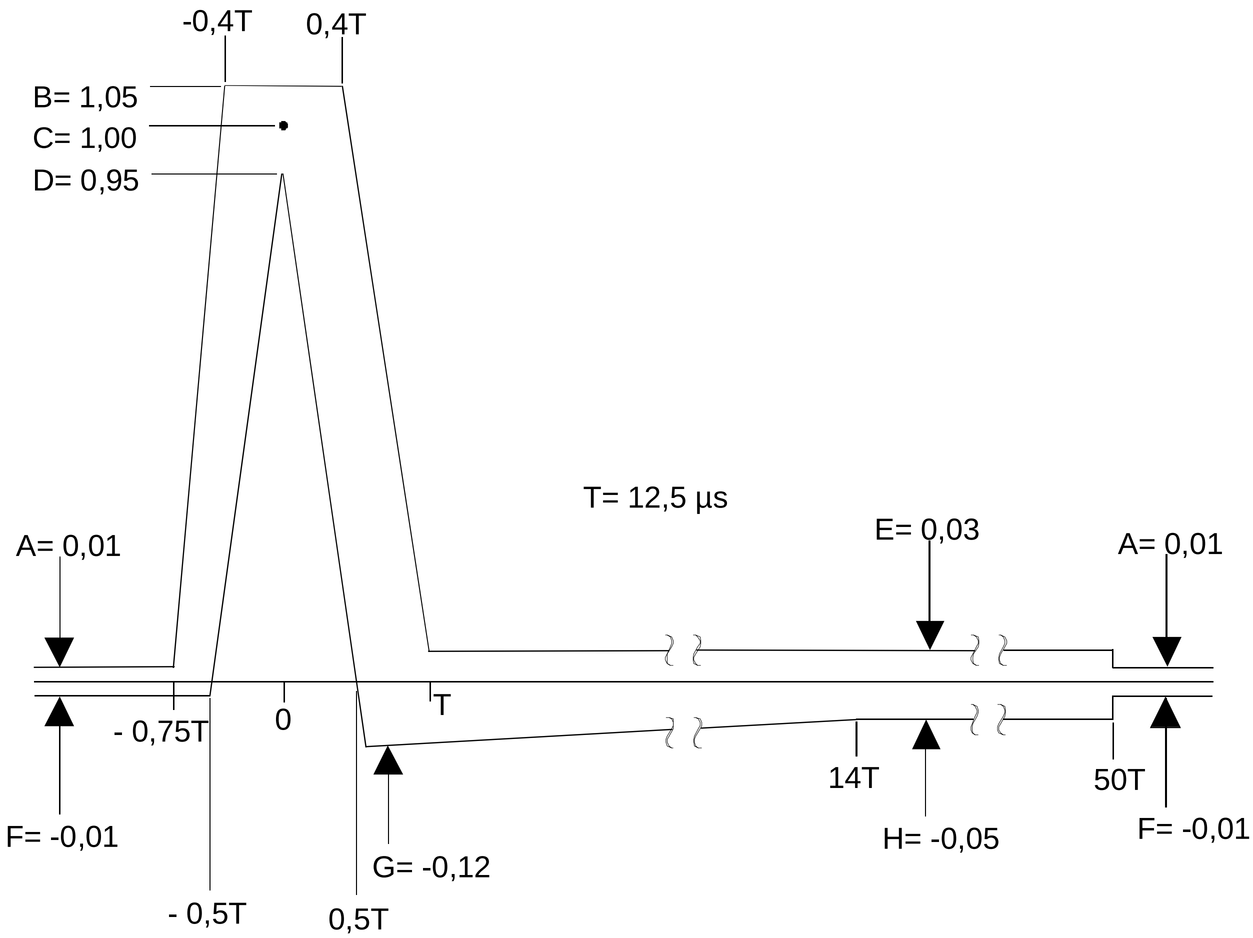
The following specifications apply with a load impedance of 135 Ω resistive over a frequency band of 100 Hz to 160 kHz.

A.12.1 Pulse amplitude

The nominal peak of the largest pulse shall be 2,5 V (see figure A.11).

A.12.2 Pulse shape

The transmitted pulse shall have the shape specified in figure A.11. The pulse mask for the four quaternary symbols shall be obtained by multiplying the normalized pulse mask shown in figure A.11 by 2,5 V, 5/6 V, -5/6 V or -2,5 V. When the signal consists of a framed sequence of symbols with a synchronization word and equiprobable symbols in all other positions, the nominal average power is 13,5 dBm.



Normalized level:		Quaternary symbols:			
		+3	**+1**	**-1**	**-3**
A	0,01	0,025 V	0,008 330 V	-0,008 330 V	-0,025 V
B	1,05	2,625 V	0,875 000 V	-0,875 000 V	-2,625 V
C	1,00	2,500 V	5/6 V	-5/6 V	-2,500 V
D	0,95	2,375 V	0,791 670 V	-0,791 670 V	-2,375 V
E	0,03	0,075 V	0,025 000 V	-0,025 000 V	-0,075 V
F	-0,01	-0,025 V	-0,008 330 V	0,008 330 V	0,025 V
G	-0,12	-0,300 V	-0,100 000 V	0,100 000 V	0,300 V
H	-0,05	-0,125 V	-0,041 670 V	0,041 670 V	0,125 V

NOTE: Compliance of transmitted pulses within boundaries of the pulse mask is not sufficient to assure compliance with the power spectral density requirement and the absolute power requirement. Compliance with the requirements in subclause A.12.3 and subclause A.12.4 is also required.

Figure A.11: Normalized output pulse from NT1 or LT

A.12.3 Signal power

The average power of a signal consisting of a framed sequence of symbols with a FW and equiprobable symbols at all other positions shall be between 13,0 dBm and 14,0 dBm over the frequency band from 100 Hz to 80 kHz.

A.12.4 Power spectral density

The upper bound of the power spectral density shall be limited according to figure A.12. Measurements to verify compliance with this requirement are to use a bandwidth of 10 kHz.

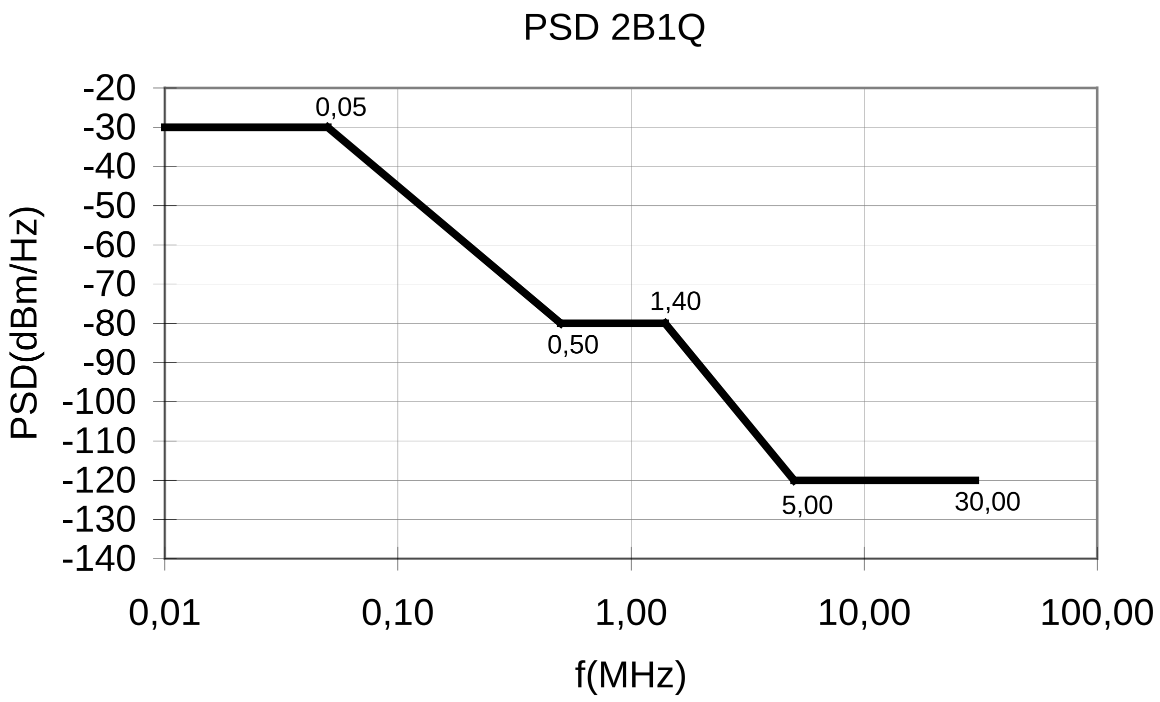


Figure A.12: Upper bound of power spectral density from NT1 and LT

Systems deployed before January 1, 2000, do not have to meet this PSD requirement but shall meet the PSD requirements as defined in ETR 080 [17]. It is however expected that these systems will also meet the PSD requirements of the present document although some narrow-band violations could occur and should be tolerated.

A.12.4.1 Sliding window PSD requirement

The purpose of the sliding window is to perform a higher bandwidth measurement in order to make sure that different systems do not fill the entire allowable band with noise up to the limit shown in figure A.12 above 300 kHz. The sliding window parameters and values are given in table A.6.

Table A.6: Sliding window parameters and values

PARAMETER	VALUE
Bandwidth of sliding window	1 MHz
Reference frequency	Lower edge
Step size	10 kHz
Start frequency	300 kHz
Stop frequency	29 MHz

The sliding window PSD shall be measured as the total average power within a 1 MHz sliding window (1MHz bandwidth). The result shall be less than -120 dBm/Hz or at least more than 10 dB below the PSD limit shown in figure A.12. The requirement is applicable between 300 kHz and 30 MHz.

Systems deployed before January 1. 2000, do not have to meet the sliding window PSD requirement.

A.12.5 Transmitter linearity

A.12.5.1 Requirements

This is a measure of the deviations from ideal pulse heights and the individual pulse non-linearity. The transmitted and received signals shall have sufficient linearity so that the residual rms non-linearity is at least 36 dB below the rms signal at the interface.

A.12.5.2 Linearity test method

With the transceiver (LT or NT1) terminated in a 135 Ω resistance through zero-length loop, and driven by an arbitrary binary sequence, the voltage appearing across the resistance is filtered (anti-alias), sampled and converted to digital form (V_{out}) with a precision of not less than 12 bits (see figure A.13). These samples are compared with the output of an adjustable, linear filter, the input of which is the scrambled, framed, and linearly encoded transmitter input. The signals at the subtractor may both be in digital form, or they may both be in analogue form.

The linear digital filter input ("quaternary input data" in figure A.13) can be considered a linearity standard. It may be produced from the transmitter output by an errorless receiver (with no descrambler), or from the scrambled transmitter input data if it is available. If the samples input to the adjustable filter are available in digital form, no additional Analogue to Digital (A/D) converter is required. Whether analogue or digital, these samples are required to be in the ratio 3:1:-1:-3, to an accuracy of at least 12 bits.

The sampling rate of the samplers and filters may be higher than the symbol rate, and generally will be several times the symbol rate for good accuracy. Alternatively, the sample rate may be at the symbol rate, but the rms values are obtained by averaging over all sample phases relative to the transmitter signal.

Because the anti-alias filter, sampler, and A/D converter operating on the transmitter output may introduce a loss or gain, proper calibration requires determining $<V_{out}^2>$ at the filter output, as shown in figure A.13, rather than the mean-squared value of the transmitter output itself.

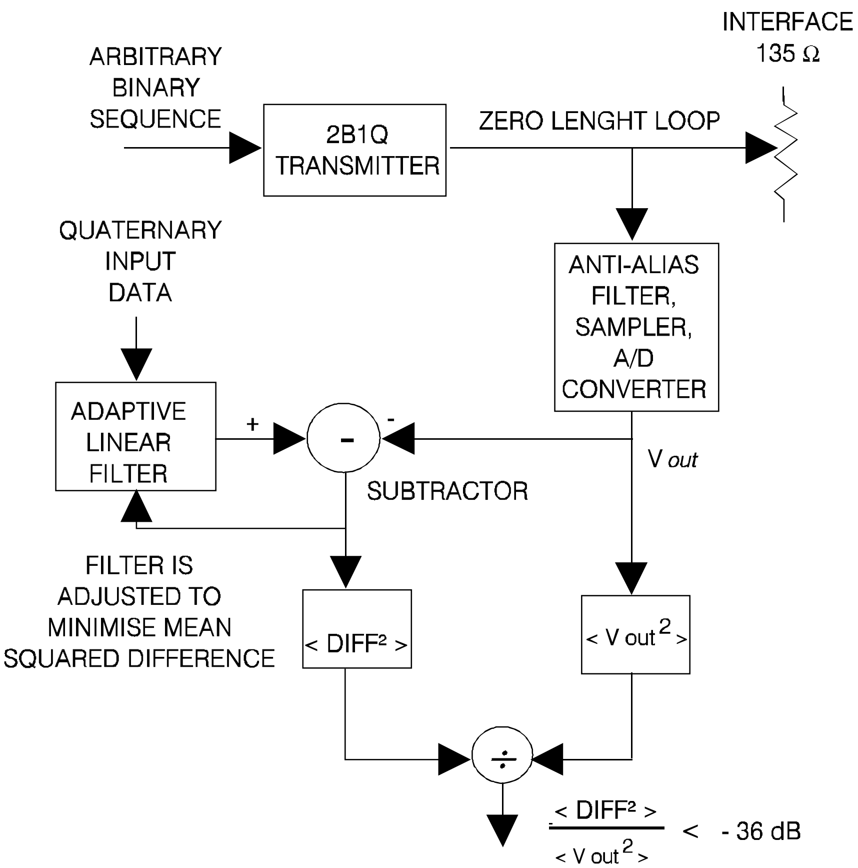


Figure A.13: Measurement of transmitter linearity

A.13 Transmitter/receiver termination

A.13.1 Impedance

The nominal driving point impedance at the interface towards the NT1, REG and LT shall be 135 Ω.

A.13.2 Return loss

The return loss with respect to 135 Ω, over a frequency band from 1 kHz to 200 kHz, shall be as shown in figure A.14.

There is no return loss requirement for the full reset and the power off state.

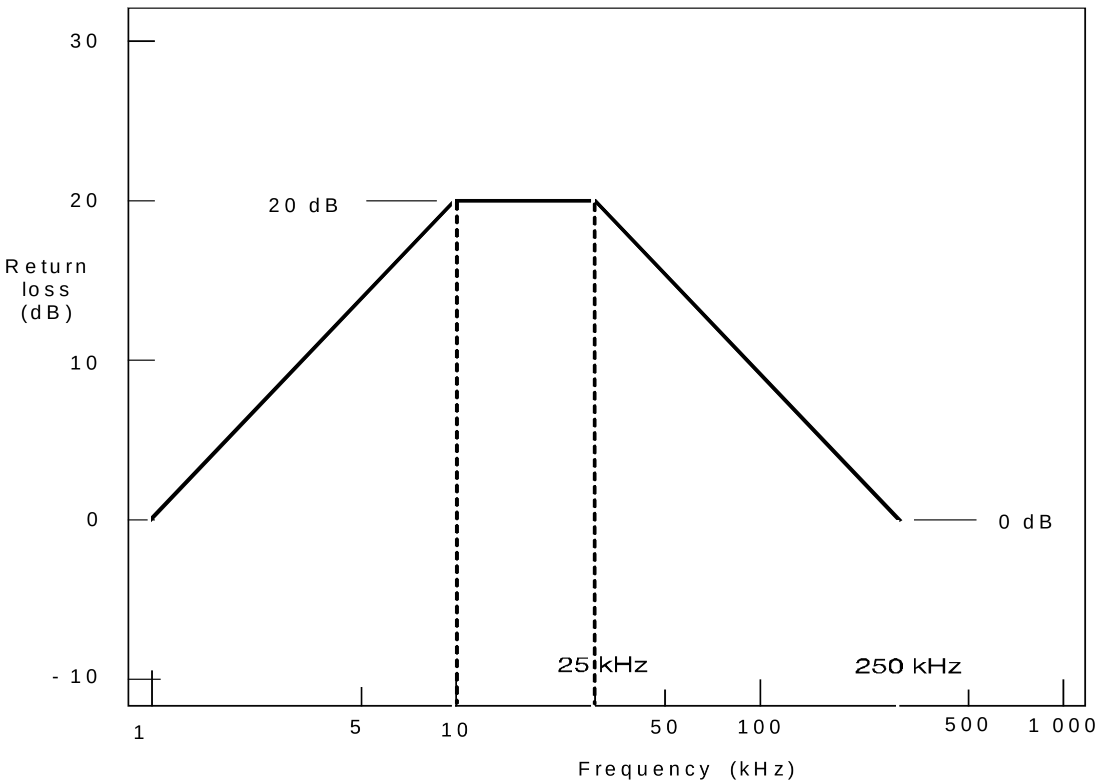


Figure A.14: Minimum return loss

A.13.3 Unbalance about earth

A.13.3.1 Longitudinal conversion loss

The Longitudinal Conversion Loss (LCL) is defined in subclause 6.3 and figure 9.

Figure A.15 gives the requirements for LCL.

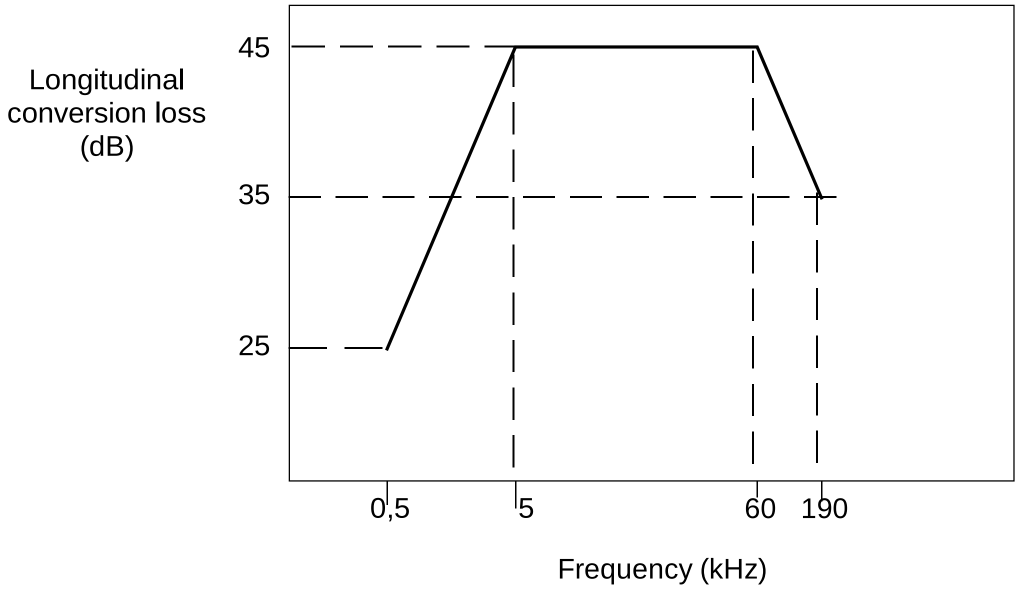


Figure A.15: Minimum longitudinal conversion loss requirement

Annex A1 (informative): Extension functions of the system using 2B1Q line code

A1.1 Introduction

The optional use of the functions as described in this annex is for information. The functions are defined in the present document.

A1.2 NT1 Power status bits

The power status bits shall be the M_4 bits in the second and third basic frames of multiframes transmitted by the NT1 (see figure A.3). The use of this function is optional. When used, the power status bits shall be used as defined in table A1.1 (see subclause A.8.3.2.4). If these bits are not used they shall be set to ONE in SN3.

Table A1.1: Power status bit assignments and messages

NT1 status	PS_1 PS_2 binary values	Definition
All Power Normal	11	Primary and back-up battery (if provided) power supplies are both normal. Normal power at T reference point, if provided.
Secondary Power Out	10	Primary power is normal, but the back-up battery (if provided) is marginal, unavailable, or has failed. Normal power at T reference point, if provided.
Primary Power Out	01	Primary power is marginal or has failed. Back-up battery (if provided) is normal. Voltage at T reference point (if provided) is less than 34 V or reversed.
Dying Gasp	00	Both primary power and back-up battery (if provided) are marginal or have failed. Voltage at T reference point (if provided) is less than 34 V or reversed. The NT1 may shortly cease normal operation.
NOTE: The coding scheme defined in this table allows several alternatives of implementation of power status provision in the NT1. Additionally, the application and the definition of the specific parameters may depend on the national network operator's maintenance strategy. The specific application and definition of parameters is, therefore, to be provided by the network operator on the basis of the general coding rule provided.		

A1.3 NTM bit

The NT1 test mode indicator bit shall be the M_4 bit in the fourth basic frame of multiframes transmitted by the NT1 to the network (see figure A.3). The use of this function is optional. The NT1 is considered to be in a test mode when the D-channel or either one of the B-channels are involved in a customer locally-initiated maintenance action. While in test mode, the NT1 may be unavailable for service or the NT1 may be unable to perform actions requested by EOC messages. If the function is used, the bit shall be a ONE to indicate normal operation and a ZERO to indicate test mode. If the function is not used, the bit shall be set to ONE in SN3 (see subclause A.8.3.2.5).

A1.4 CSO bit

The Cold-Start-Only (CSO) bit is the M_4 bit in the fifth frame of the multiframe transmitted by a NT1. The use of this function is optional. It may be used to indicate the start-up capabilities of the NT1 transceiver. If the NT1 has a cold-start-only transceiver, as defined in clause A.10 (5), this bit is set to ONE. Otherwise, this bit shall be set to ZERO in SN3 (see subclause A.8.3.2.6).

A1.5 UOA bit

The DLL-Only-Activation (UOA) bit shall be the M_4 bit in the seventh basic frame of the multiframes transmitted by a LT. The use of this function is optional. If used, it shall be used to request the NT1 to activate or deactivate the interface at the T reference point (if present). If the interface at the T reference point is to be activated, this bit may be set to ONE. Otherwise, this bit shall be set to ZERO. If the function is not used, the bit shall be set to ONE in SL2 and SL3 (see subclause A.8.3.2.7). Tables A1.2 and A1.3 are state transition tables showing the use of the UOA bit in activation of the DLL without activating the interface at the T reference point. Figures A1.3 through A1.7 illustrate these examples further.

A1.6 SAI bit

The S/T-interface-Activity-Indicator (SAI) bit shall be the M_4 bit in the seventh basic frame of the multiframes transmitted by a NT1. The use of this function is optional. If used, it shall be used to indicate to the network when there is activity at the interface at the T reference point. If there is activity (INFO 1 or INFO 3) at the interface at the T reference point, this bit shall be set to ONE. Otherwise it shall be set to ZERO. If this function is not used, the bit shall be set to ONE in SN3 (see subclause A.8.3.2.8). This bit may be used in conjunction with DLL-only-activation; see clause A1.5.

A1.7 AIB

The Alarm Indicator Bit (AIB) shall be the M_4 bit in the eighth basic frame of the multiframes transmitted by the network towards the NT1. The use of this function is optional. When the transmission path for D-channel, B_1-channel, and B_2-channel has been established all the way to the local exchange, a ONE may be forwarded to the NT1. Failure or interruption of an intermediate transmission system which transports the D-channel, B_1-channel, and B_2-channel shall result in forwarding ZERO to the NT1. Such failures may include loss of signal, loss of frame synchronization/carrier link or basic access DLL, and transmission terminal failure. Intermediate transmission interruptions may include loopbacks at intermediate points or absence of provisioning of an intermediate transmission system. If this function is not used, the bit shall be set to ONE in SN3 (see subclause A.8.3.2.9).

Table A1.2: Activation/deactivation: NT finite state matrix (DSL-only turn-on option): an example

Event ↓	Power off	Full reset	Alerting	EC Training (optional)	EC converged	FW sync	IFW sync	IFW sync CALL	Pending active	Active	UOA	S/T deacti-vation	UOA & TE CALL	Pending deacti-vation	Tear down	Receive reset
State name	**Power off**	**Full reset**	**Alerting**	**EC Training (optional)**	**EC converged**	**FW sync**	**IFW sync**	**IFW sync CALL**	**Pending active**	**Active**	**UOA**	**S/T deacti-vation**	**UOA & TE CALL**	**Pending deacti-vation**	**Tear down**	**Receive reset**
State code (figure A.6 event)	**NT0**	**NT1 (T0)**	**NT2**	**NT3 (T1)**	**NT4 (T2)**	**NT5 (T5)**	**NT6(a) (T6)**	**NT6 (T6)**	**NT7**	**NT8**	**NT8(a)**	**NT8(b)**	**NT8(c)**	**NT9**	**NT10**	**NT12**
Signal → LT	**SN0**	**SN0**	**TN**	**SN1**	**SN0**	**SN2**	**SN3 act=0 sal=1 or 0**	**SN3 act=0 sal=1 or 0**	**SN3 act=1 sal=1**	**SN3 act=1 sal=1**	**SN3 act=0 sal=0**	**SN3 act=0 sal=0**	**SN3 act=0 sal=1**	**SN3 (note 8)**	**SN0**	**SN0**
Signal → TE	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 2**	**INFO 2**	**INFO 4**	**INFO 0**	**INFO 0**	**INFO 0**		**INFO 0**	**INFO 0**
Power ON	NT1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Loss of power	-	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0	NT0
Received new S/T INFO 1 signal (note 2)	/	ST.M4 NT2 (note 12)	-	-	-	-	-	-	/	/	NT8(c)	NT8(c)	-	-	-	-
Received INFO 3 signal (uoa=1, act=0, dea=1) (note 2)	/	/	/	/	/	/	/	NT7	-	-	/	-	/	-	-	-
Received INFO 0 or S/T Loss of Sync (note 2)	/	-	-	-	-	-	-	-	NT6	NT6	/	NT8(a)	/	-	-	-
End of tone TN (9 ms)	/	/	NT3 or NT4	/	/	/	/	/	/	/	/	/	/	/	/	/
Received tone TL	/	ST.M4 NT2	-	/	/	/	/	/	/	/	/	/	/	/	/	STP.M6 NT2
Echo canceller converged	/	-	-	NT4	-	-	-	-	-	-	-	-	-	-	-	-
FW sync and detect SL2	/	/	/	/	NT5	-	-	-	-	-	-	-	-	-	-	/
IFW sync (SL2)	/	/	/	/	/	STP.M4 NT6(a)	-	-	-	-	-	-	-	-	-	/
Received (SL2 or SL3) dea=0 (note 6)	/	/	/	/	/	/	NT9	NT9	NT9	NT9	NT9	NT9	NT9	-	-	/
Received (SL2 or SL3) uoa=0 and dea=1	/	/	/	/	/	/	NT8(a) or NT8(c)	NT8(a) or NT8(c)	NT8(b)	NT8(b)	-	-	-	Previous state (note 13)	-	/

Event ↓	State name	Power off	Full reset	Alerting	EC Training (optional)	EC converged	FW sync	IFW sync	IFW sync CALL	Pending active	Active	UOA	S/T deacti-vation	UOA & TE CALL	Pending deacti-vation	Tear down	Receive reset
	State code (figure A.6 event)	**NT0**	**NT1 (T0)**	**NT2**	**NT3 (T1)**	**NT4 (T2)**	**NT5 (T5)**	**NT6(a) (T6)**	**NT6 (T6)**	**NT7**	**NT8**	**NT8(a)**	**NT8(b)**	**NT8(c)**	**NT9**	**NT10**	**NT12**
	Signal → LT	**SN0**	**SN0**	**TN**	**SN1**	**SN0**	**SN2**	**SN3 act=0 sal=1 or 0**	**SN3 act=0 sal=1 or 0**	**SN3 act=1 sal=1**	**SN3 act=1 sal=1**	**SN3 act=0 sal=0**	**SN3 act=0 sal=0**	**SN3 act=0 sal=1**	**SN3 (note 8)**	**SN0**	**SN0**
	Signal → TE	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 2**	**INFO 2**	**INFO 4**	**INFO 0**	**INFO 0**	**INFO 0**		**INFO 0**	**INFO 0**
Received (SL2 or SL3) uoa=1, act=0 and dea=1		/	/	/	/	/	/	NT6	-	-	NT7	NT6	-	NT6	Previous state (note 13)	-	/
Received (SL3) uoa=1, act=1 and dea=1		/	/	/	/	/	/	-	-	NT8	-	-	-	-	Previous state (note 13)	-	/
Loss of synchronization (> 480 ms)		/	/	/	/	/	/	NT10	NT10	NT10	NT10	NT10	NT10	NT10	NT10	-	-
Loss of signal (> 480 ms)		/	/	/	/	STP.M4 NT1 (note 14)	-	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	ST.M6 NT12	/	/	-
Expiry of timer M4 (15 seconds)		/	/	/	NT10	NT10	NT10	/	/	/	/	/	/	/	/	/	-
Loss of signal < 40 ms		/	/	/	/	-	-	-	-	-	-	-	-	-	ST.M6 NT12	ST.M6 NT12	/
Expiry of timer M6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	NT1

NOTE: For symbols and abbreviations, see table A1.4.

Table A1.3: Activation/deactivation: LT finite state matrix (DSL-only turn-on option): an example

State name	Power off	Full reset	Alerting	Awake	EC Training (optional)	EC converged CALL	FW sync CALL	IFW sync CALL	Active	EC converged UOA	FW sync UOA	U active	Deactivation S/T	Deactivation alerting	Tear down	Pending deactivation	Receive reset
State code (figure A.6 event)	LT0	LT1 (T0)	LT2	LT3 (T1)	LT4 (T3)	LT5 (T4)	LT6	LT7 (T7)	LT8	LT5(a) (T4)	LT6(a)	lT8(a)	LT7(a)	LT9	LT10	LT11	LT12
Event ↓ / Signal → NT	SL0	SL0	TL	SL0	SL1	SL2 dea=1 act=0 uoa=1	SL2 dea=1 act=0 uoa=1	SL3 dea=1 act=0 uoa=1	SL3 dea=1 act=1 uoa=1	SL2 dea=1 act=0 uoa=0	SL2 dea=1 act=0 uoa=0	SL3 dea=1 act=0 uoa=0	SL3 dea=1 act=0 uoa=0	SL3 dea=0 act=0	SL0	SL0	SL0
Power ON	LT1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Loss of power (note 1)	-	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7	LT0 FE7
Activation request (FE1) (note 1)	-	ST.M5 LT2 FE2	-	-	-	-	-	-	-	LT5	LT6	LT7	LT7	-	-	-	-
U-only Turn-on request (FE11) (note 1)	-	ST.M5 LT2	-	-	-	LT5(a)	LT6(a)	LT7(a)	LT7(a)	-	-	-	-	-	-	-	-
Deactivation request (FE5) (notes 1 and 9)	-	-	-	-	-	-	-	LT9	LT9	-	-	LT9	LT9	-	-	-	-
End of tone TL (3 ms)	/	/	LT3	/	/	/	/	/	/	/	/	/	/	/	/	/	/
Received tone TN	/	ST.M5 LT3 FE2	-	-	/	/	/	/	/	/	/	/	/	/	/	/	ST.M5 STP.M7 LT3 FE2
Loss of signal energy (TN or SN1)	/	-	-	LT4, LT5 or LT5(a)	-	/	/	/	/	/	/	/	/	/	/	/	/
Echo canceller converged and FE11 (note 1)	/	-	-	-	LT5(a)	-	-	-	-	-	-	-	-	-	-	-	-
Echo canceller converged and FE1 (note 1)	/	-	-	-	LT5	-	-	-	-	-	-	-	-	-	-	-	-
FW sync (SN2 or SN3)	/	/	/	/	/	LT6	-	-	-	LT6(a)	-	-	-	-	-	-	-

	State name	**Power off**	**Full reset**	**Alerting**	**Awake**	**EC Training (optional)**	**EC converged CALL**	**FW sync CALL**	**IFW sync CALL**	**Active**	**EC converged UOA**	**FW sync UOA**	**U active**	**Deacti-vation S/T**	**Deacti-vation alerting**	**Tear down**	**Pending deacti-vation**	**Receive reset**
	State code (figure A.6 event)	**LT0**	**LT1 (T0)**	**LT2**	**LT3 (T1)**	**LT4 (T3)**	**LT5 (T4)**	**LT6**	**LT7 (T7)**	**LT8**	**LT5(a) (T4)**	**LT6(a)**	**lT8(a)**	**LT7(a)**	**LT9**	**LT10**	**LT11**	**LT12**
Event ↓	**Signal → NT**	**SL0**	**SL0**	**TL**	**SL0**	**SL1**	**SL2 dea=1 act=0 uoa=1**	**SL2 dea=1 act=0 uoa=1**	**SL3 dea=1 act=0 uoa=1**	**SL3 dea=1 act=1 uoa=1**	**SL2 dea=1 act=0 uoa=0**	**SL2 dea=1 act=0 uoa=0**	**SL3 dea=1 act=0 uoa=0**	**SL3 dea=1 act=0 uoa=0**	**SL3 dea=0 act=0**	**SL0**	**SL0**	**SL0**
IFW sync (SN3) (note 1)		/	/	/	/	/	/	STP.M5 LT7 FE3	-	-	/	STP.M5 LT8(a) FE3	-	-	-	-	-	-
Received (SN3) act=0 (note 1)		/	/	/	/	/	/	/	-	LT7 FE12	/	/	-	LT8(a) FE3	-	-	-	-
Received (SN3) act=1 (note 1)		/	/	/	/	/	/	/	LT8 FE4	-	/	/	/	-	-	-	-	-
Received (SN3) sal=1 (note 1)		/	/	/	/	/	/	/	-	-	/	/	LT7 FE2 (note 15)	-	-	-	-	-
Loss of synchronization (> 480 ms) (note 1)		/	/	/	/	/	/	/	LT10 FE7	LT10 FE7	/	/	LT10 FE7	LT10 FE7	LT10 FE7	-	-	-
Loss of signal (> 480 S) (note 1)		/	/	/	LT1	/	-	-	ST.M7 LT12 FE7	ST.M7 LT12 FE7	-	-	ST.M7 LT12 FE7	ST.M7 LT12 FE7	ST.M7 LT12 FE7	-	-	-
End of last super frame with dea=0 (note 10)		/	/	/	/	/	/	/	/	/	/	/	/	/	LT11	/	/	/
Expiry of timer M5 (15 seconds) (note 1)		/	/	/	LT10 FE7	LT10 FE7	LT10 FE7	LT10 FE7	/	/	LT10 FE7	LT10 FE7	/	/	/	/	/	/
Absence of signal < 40 ms (note 1)		/	-	/	/	/	-	-	-	-	-	-	-	-	-	ST.M7 LT12	LT1 FE6	-
Expiry of timer M7 (40 ms) (note 1)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	LT1 FE6

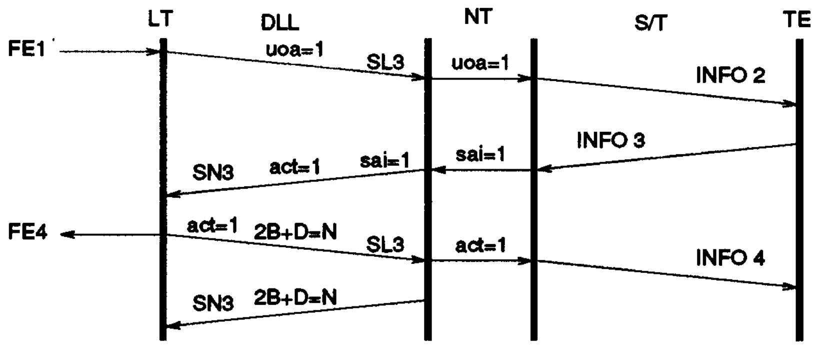
NOTE: For symbols and abbreviations, see table A1.4.

Table A1.4: Symbols, abbreviations and notes for tables A1.2 and A1.3

Symbols, abbreviations and notes for tables A1.2 and A1.3		
Symbols and abbreviations:		
"-"	=	No change, no action.
"/"	=	Impossible or prohibited situation under normal circumstances.
"FE1"	=	Activate Access Request (AR) (note 1).
"FE2"	=	Access Activation Initiated (note 1).
"FE3"	=	Line Transceivers Activated (note 1).
"FE4"	=	Access Activated or Loopback Operated (AI) (note 1).
"FE5"	=	Deactivate Access Request (note 1).
"FE6"	=	Access or Loopback Deactivated (DI) (note 1).
"FE7"	=	LOS/LFA in Line Transceivers - (including Loss of Power at NT1) (note 1).
"FE8"	=	Activate Loopback 2 (note 1).
"FE9"	=	Activate Loopback 1 (at LT towards network) (note 1).
"FE10"	=	Activate Loopback 1a (at Regenerator towards network) (note 1).
"FE11"	=	Partial Activation Request (UOA) (see subclause A.8.3.2.7) (note 1).
"FE12"	=	Report LOS/LFA at T reference point (see subclause A.8.3.2.8).
"FE13"	=	Deactivate the interface at T reference point whilst keeping the Access Digital Section activated (note 1).
"NTn"	=	Go to state "NTn".
"LTn"	=	Go to state "LTn".
"ST.Mn"	=	Start timer Mn.
"STP.Mn"	=	Stop timer Mn.
"SLn,SNn"	=	Signals defined in figures A.6 and A.7 (SL0, SN0 = no signal).
"Tn"	=	Events defined in figures A.6 and A.7.

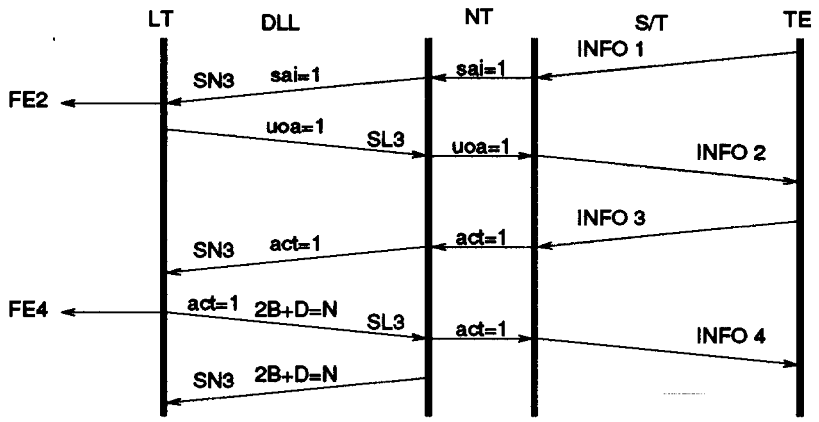
NOTES:

NOTE 1: The function elements are also defined in subclause 8.4.3 of ETS 300 297 [4].
NOTE 2: INFO signals at the T reference point are defined in subclause A.6.2.2 of ETS 300 012 [1].
NOTE 3: Void.
NOTE 4: Void.
NOTE 5: Void.
NOTE 6: Cold-start-only NTs may ignore this event.
NOTE 7: Void.
NOTE 8: The signals output in this state remain unchanged from signals output during the preceding state (for example, ACT=0 if state NT6 preceded, or ACT=1 if states NT7 or NT8 preceded). The INFOs also remain unchanged.
NOTE 9: This event is only the first step of a sequence leading to deactivation. After transmitting DEA=0 for a short interval (see note 10), the LT sends SL0 to deactivate the NT.
NOTE 10: This event occurs as a result of FE5 (see note 9) after entering state LT9 and transmitting at least three super frames with DEA=0 (see subclause A.10.1.5).
NOTE 11: Void.
NOTE 12: When INFO 1 remains continuous after the NT fails to bring up the network side and returns to state NT1, the NT does not go again into state NT2 unless a new transition from INFO 0 to INFO 1 is received (see clause A.10 (10) and ETS 300 012 [1]).
NOTE 13: The transceiver should return to the state from which it entered state NT9, unless the UOA or ACT bit(s) have changed.
NOTE 14: The transitions resulting from this event, to either full reset (NT1) or receive reset (NT12), are controlled by the requirements in subclause A.10.2.
NOTE 15: The network is permitted to choose "No action" rather than sending FE1 and transferring to state LT7. For example, when the access link is undergoing maintenance, "No action" is an appropriate response.



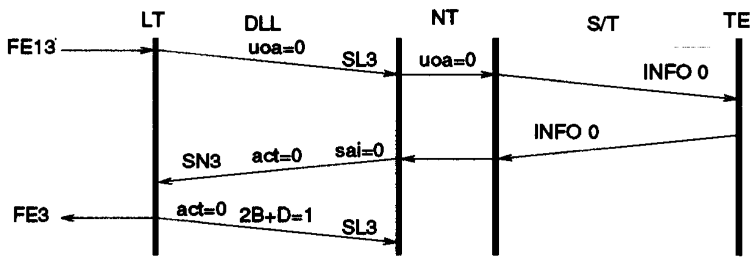
NOTE 1: Receipt of INFO3 and SL3 at the NT can theoretically occur in either order.
NOTE 2: For symbols and abbreviations see table A1.4.

Figure A1.1: Change from DSL-only to total activation initiated by the exchange (FE1)



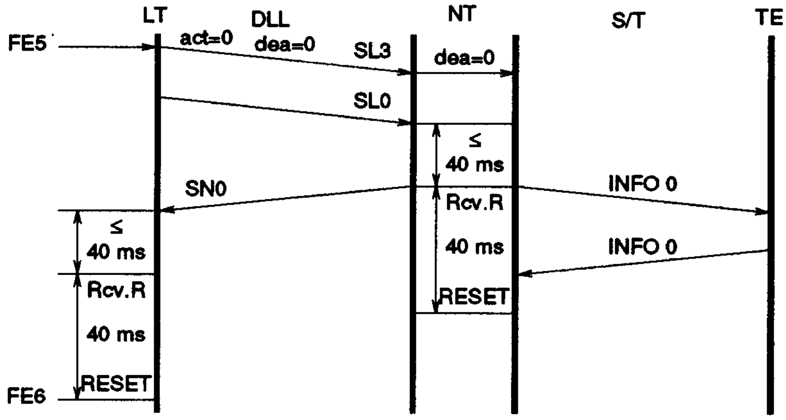
NOTE 1: Receipt of INFO3 and SL3 at the NT can theoretically occur in either order.
NOTE 2: For symbols and abbreviations see table A1.4.

Figure A1.2: Change from DSL-only to total activation initiated by terminal equipment (INFO 1)



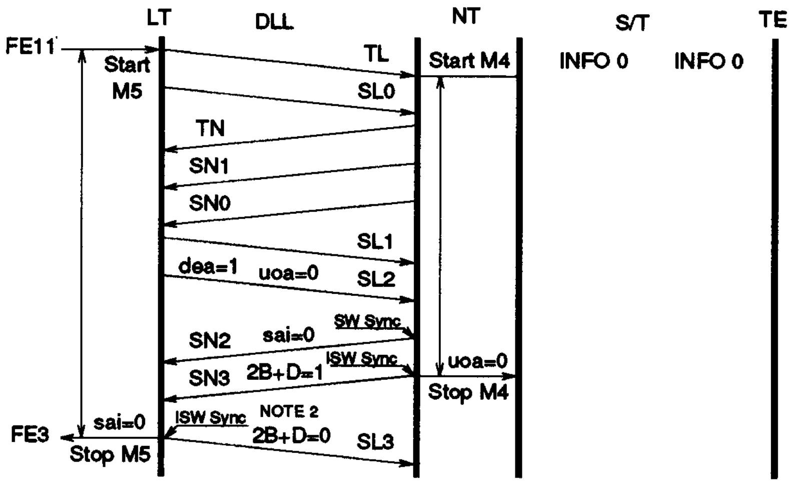
NOTE: For symbols and abbreviations see table A1.4.

Figure A1.3: Change to DSL-only from total activation initiated by the exchange (FE13)



NOTE 1: For symbols and abbreviations see table A1.4.

Figure A1.4: Total deactivation process



NOTE 1: For symbols and abbreviations see table A1.4.
NOTE 2: Except to perform a loopback, 2B+D bits shall remain in the previous state (SN2 or SL2) until both act bits indicate full transparency of B-channels and D-channels (see figure A.7). Transparency required to perform loopbacks is independent of the act bits.

Figure A1.5: DSL-only turn-on process initiated by the exchange from reset (FE11)

Annex A2 (informative): Discussion of EOC addressing

Figure A2.1 shows a possible worst-case architecture for supporting ISDN basic access. In such extended configurations, the Digital Subscriber Line (DSL) provided by the switch connects to intermediate transmission equipment instead of connecting directly to a NT. There may be additional transmission elements at more distant points in the configuration before eventually terminating at the NT.

Each transmission element indicated by **n** in clause A2.1, with **n** equal to 1 through 5, may need to be given an EOC address. This allows the switch to send layer-1 maintenance commands to each of these elements. The address for such transmission elements is assigned in a relative fashion with respect to the switch, such that the first element from the switch is treated by the network as EOC address 1, the next as EOC address 2, and so on. The NT is always addressed as 0.

A2.1 Addresses 1 through 6 (intermediate elements)

For the addressing scheme, the intermediate transmission element have EOC addresses in the range of 1 to 6. Intermediate transmission elements will react to addresses 1 through 6 as follows:

a) direction towards customer (network to NT):

1) if address in range of 2 to 6, decrement address and pass message on;

2) if address equals 1, comply with received message and send proper EOC response frame back towards the network. The response frame will be written over the response frame from the NT. Pass the EOC frame on with the broadcast address and the message changed to hold state;

b) direction towards network (NT to network):

- if address in range 1 to 5, increment address and pass message on.

NOTE: For the addressing mechanism described in this annex, the order of the address bits in the EOC address field is important. In figure A.3 the M_1, M_2 and M_3 bits in the first frame of the multiframe are the eoc address, EOC_{a1}, EOC_{a2} and EOC_{a3}, respectively. In this address field, EOC_{a3} is the least significant bit.

A2.2 Action of intermediate elements

The intermediate transmission elements will react to EOC addresses 0 and 7 (NT address and broadcast address, respectively) as follows:

a) if address 0, address not changed and message passed on (both directions);

b) if address 7, comply with received message, address not changed, and message passed on (both directions).

Therefore, all downstream units would comply with a message with a broadcast address; however, only the NT would respond with an acknowledgement. Intermediate units would relay the NT's acknowledgement to the network.

When EOC messages for internal ISDN network use activate operations functions identical to operations functions standardized at the NT, then the message codes for those messages should also be identical.

A2.3 Action of NT

The NT will only comply with messages to addresses 0 and 7. When messages are received at the NT with addresses 1 through 6, the NT sends back an EOC frame with the hold state message and address 0. The proper action for the NT in every case is fully defined in subclause A.8.3.3.2.

A2.4 Summary

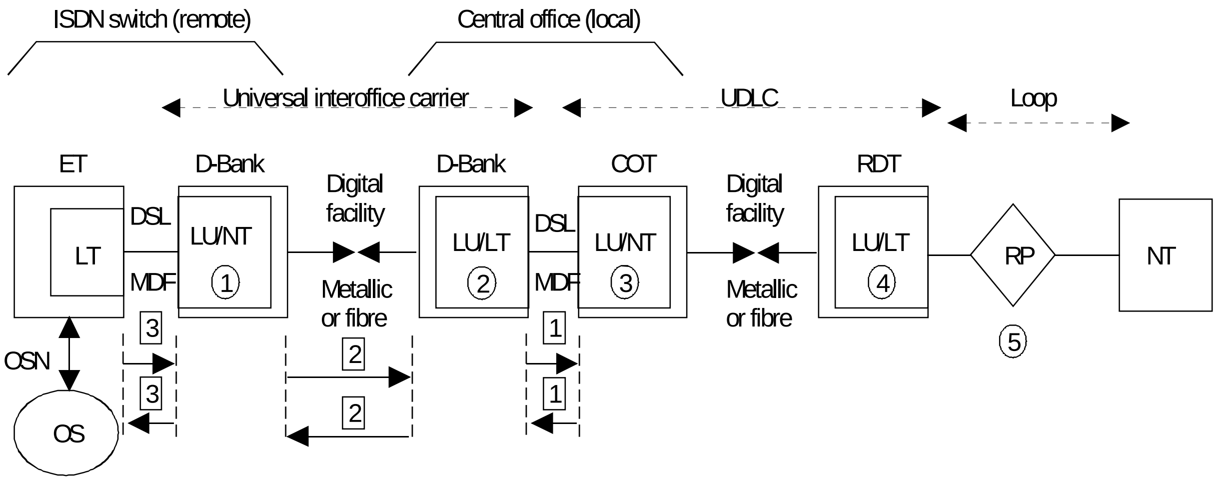
The above addressing scheme for assigning EOC addresses to intermediate transmission elements of extended configurations allows maintenance functions to be performed at each element, simplifying circuit provisioning and minimizing network reconfiguration costs.

Figure A2.1 shows an example of a loopback request for element No 3 and the value of the address field at different links in the circuit.

In using this addressing scheme, it is important for the network to be aware of the exact configuration. Otherwise, the network may fail to address elements that are present, or may attempt to address elements that are not present. In any case, by not having correct information about the configuration, the network may send and receive data or issue commands that have entirely different meaning or results than expected.

The network will become aware of the fact that it is addressing an intermediate element beyond the last intermediate element in the configuration, because the NT will reply with the 0 address and the hold state message, However, if the actual configuration has more elements than assumed by the network, none of the messages sent by the network to intermediate addresses will result in a reply with a 0 address.

The NT response to messages it receives, that are not addressed to it, provides a means of determining the correct configuration at any time. The determination is possible because the network receives EOC frames with the address 0 and the hold state message, when it addresses a non-existent element. For example, the correct EOC configuration may be determined at any time by the network, sending the hold state message with EOC address first set to 1, and then set to successively higher addresses until address 0 is returned in three consecutive identical EOC frames. This procedure can eliminate confusion and assure accurate communication on the EOC channel in those cases when record errors would have led to confusion. If record errors are a problem, or changes of configuration are frequent, this procedure may be repeated often enough to assure valid results of EOC transactions.



Symbols and abbreviations:

COT	= Central Office Terminal	n	= nth transmission element
DSL	= Digital Subscriber Line	NT	= Network Termination
ET	= Exchange Termination	OS	= Operations System
D-Bank	= Digital channel Bank/multiplexer	OSN	= Operations System Network (packet)
LT	= Line Termination	RDT	= Remote Digital Terminal
LU/LT	= Line Unit/LT	RP	= Loop Repeater, network
LU/NT	= Line Unit/NT	UDLC	= Universal Digital Loop Carrier
MDF	= Main Distribution Frame	x	= Message with address x

Figure A2.1: Worst case ISDN basic access configuration

Annex B (normative): Definition of a system using Modified Monitoring State (MMS) 43 line code

B.1 Line code

For each direction of transmission, the line code shall be the Modified Monitoring State (MMS) code mapping 4 bits into 3 ternary symbols with levels +, 0 or - (MMS 43). Details of the coding scheme are given in figure B.1. Note that the numbers in the columns for each of the 4 alphabets S1... S4 give the numbers of the alphabet to be used for the coding of the next block of 4 bits. The bits and symbols on the left are those transmitted or received first.

	S1				S2				S3				S4			
0001	0	-	+	1	0	-	+	2	0	-	+	3	0	-	+	4
0111	-	0	+	1	-	0	+	2	-	0	+	3	-	0	+	4
0100	-	+	0	1	-	+	0	2	-	+	0	3	-	+	0	4
0010	+	-	0	1	+	-	0	2	+	-	0	3	+	-	0	4
1011	+	0	-	1	+	0	-	2	+	0	-	3	+	0	-	4
1110	0	+	-	1	0	+	-	2	0	+	-	3	0	+	-	4
1001	+	-	+	2	+	-	+	3	+	-	+	4	-	-	-	1
0011	0	0	+	2	0	0	+	3	0	0	+	4	-	-	0	2
1101	0	+	0	2	0	+	0	3	0	+	0	4	-	0	-	2
1000	+	0	0	2	+	0	0	3	+	0	0	4	0	-	-	2
0110	-	+	+	2	-	+	+	3	-	-	+	2	-	-	+	3
1010	+	+	-	2	+	+	-	3	+	-	-	2	+	-	-	3
1111	+	+	0	3	0	0	-	1	0	0	-	2	0	0	-	3
0000	+	0	+	3	0	-	0	1	0	-	0	2	0	-	0	3
0101	0	+	+	3	-	0	0	1	-	0	0	2	-	0	0	3
1100	+	+	+	4	-	+	-	1	-	+	-	2	-	+	-	3

NOTE: A received ternary block 000 is decoded as binary 0000.

Figure B.1: MMS 43-code

B.2 Symbol rate

The symbol rate shall be 120 kbaud.

B.2.1 Clock symbol requirements

B.2.1.1 NT1 free running clock accuracy

The tolerance of the free running NT1 clock shall be ± 100 ppm.

B.2.1.2 LT clock tolerance

The tolerance of the clock signal provided by the LT shall be ± 32 ppm with a frequency drift of < 5 x 10^{-7} per day.

B.3 Frame structure

Each frame contains a frame word, 2B + D data and the C_L channel. Multiframes are not used.

B.3.1 Frame length

The length of each frame shall be 120 ternary symbols corresponding to 1 ms. Each frame has 108 symbols (corresponding to 144 bits) carrying 2B + D data.

B.3.2 Symbol allocation LT to NT1

In the direction LT to NT1, the 120 symbols of each frame are used as follows:

- symbols 1 to 84: 2B+D;
- symbol 85: C_L-channel;
- symbols 86 to 109: 2B+D;
- symbols 110 to 120: frame word.

The channel allocation to the symbols 1 to 84 and 86 to 109 and the structure of the frame shall be as follows:

- 8 consecutive blocks of B_1+B_2+D, in total 144 bits, shall be scrambled and coded into 108 ternary symbols according to figure B.1. The first $\mathbf{B_1}$ channel shall start with symbol number 1;
- after 84 of such coded symbols, the C_L channel symbol shall be inserted, continued with the remaining 24 coded symbols. The 11 symbols forming the frame word shall be added after symbol 109.

B.3.3 Symbol allocation NT1 to LT

In the direction NT1 to LT, the frame structure shall be identical to that of the direction LT to NT1.

The frame transmitted by the NT1 shall be synchronized to that received from the LT.

B.4 Frame word

B.4.1 Frame word in direction LT to NT1

The frame word in the direction LT to NT1 shall be:

+ + + - - - + - - + -

B.4.2 Frame word in direction NT1 to LT

The frame word in the direction NT1 to LT shall be:

- + - - + - - - + + +

B.5 Frame alignment procedure

The transmission system shall be considered to be synchronous if the frame word has been identified in the same position for 4 immediately succeeding frames. Loss of synchronization shall be assumed if the detected frame position does not coincide with the expected position during 60... 200 successive frames.

B.6 Multiframe

Void.

B.7 Frame offset at NT1

On the line at the NT1, the frame word transmitted by the NT1 occurs 60 ± 1 symbols (0,5 ms) later than that received at the NT1 input, measured between the first symbols of each frame word.

B.8 C_L channel

B.8.1 Bit rate

The bit rate for the C_L channel (maintenance-channel) shall be 1 kbit/s.

B.8.2 Structure

No specific structure is defined for transparent messages.

B.8.3 Protocols and procedures

Transparent messages in the C_L channel use "0" and "-" polarity of the C_L symbol of the line signal. "0" and "+" polarity are used to request a loopback 2B+D in the NT1 or an intermediate repeater. Transparent use of the C_L channel may override these loopback commands.

Continuous "0" polarity shall be used as idle code.

The command/information channel protocol shall use "0" and "+" polarity codings.

Loopback commands are coded as follows:

- Loopback 1A activation (in regenerator): continuous "+0";
- Loopback 2 activation (in NT1): continuous "+";
- Loopback deactivation: continuous "0".

An activation or deactivation command shall be identified when 8 consecutive symbols according to the coding rule have been detected.

Transmission error detection and report:

- transmission errors shall be detected by monitoring frames received with one or more line code violations. An errored frame detected by the NT1 shall be reported back to the LT by setting one C_L symbol to "+" polarity.

Transparent channel:

- the transparent channel shall use "-" polarity for ZERO, "0" and "+" polarity shall be interpreted as ONE. "0" or "+" polarity shall be considered as idle code.

Messages of the transparent channel shall have priority.

B.9 Scrambling

In order to minimize correlation between incoming and transmitted symbols scrambling shall be used. Scrambling shall be applied only to the 2B+D channels.

The scrambling polynomial shall be different in both NT1 to LT and LT to NT1 directions:

- in direction LT to NT1: $1 \oplus x^{-5} \oplus x^{-23}$;
- in direction NT1 to LT: $1 \oplus x^{-18} \oplus x^{-23}$.

where $\oplus$ is the modulo two sum and x^{-k} is the scrambled data delayed by k symbol intervals.

B.10 Activation/deactivation

Activation/deactivation shall be provided to enable the use of a power down state, especially for applications where the NT1 shall be powered from the LT via the local line. Activation from the power state may be initiated from both ends using a 7,5 kHz burst signal. Collisions are handled through appropriate duration and repetition rate of these bursts.

The procedures on the line system support the procedures at reference point T for call control in accordance with ETS 300 012 [1] and the operation of loopbacks 1 (in the LT), 1A (in the regenerator) and 2 (in the NT1). The loopbacks are transparent.

Timer 1 and timer 2, as defined in ETS 300 012 [1], are located as follows:

- timer 1 in the ET layer 1 or the ET;
- timer 2 in the NT1.

The activation of the line system for maintenance purposes, e.g. error performance monitoring, shall be possible, even if no TE is connected to the interface at T reference point.

Transmission of INFO 2 on the interface of T reference point shall be initiated when the line system is synchronized in the direction LT to NT1.

B.10.1 Signals used for activation

To provide means to control/indicate progress during activation/deactivation across the local line the following signal elements are used:

SIG 0 NT1 to LT and LT to NT1

No signal.

SIG 1W NT1 to LT

Awake signal (7,5 kHz tone), signals the layer 1 entity in the local exchange that it has to enter the power-up state and provide for the activation of the line system and the interface at T reference point. This signal shall also be used as awake acknowledge on the receipt of SIG 2W.

SIG 2W LT to NT1

Awake signal (7,5 kHz tone) signals the NT1 that it shall enter the power-up state and prepare for synchronization on an incoming signal from the LT. This signal shall also be used as awake acknowledge on the receipt of SIG 1W.

SIG 1 NT1 to LT

Signal which contains framing information and allows the synchronization of the receiver in the LT. It informs the LT that the NT1 has synchronized on SIG 2.

SIG 2 LT to NT1

Signal which contains framing information and allows the synchronization of the receiver in the NT1.

SIG 1A NT1 to LT

Signal similar to SIG 1 but without framing information.

SIG 3 NT1 to LT

Signal which contains framing information and allows the synchronization of the receiver in the LT. It indicates to the ET that the interface at T reference point shall be synchronized in both directions of transmission (except in the case of loopback 2 and 1A).

SIG 4H LT to NT1

Signal which requires the NT1 to establish full layer 1 information transfer capability in both directions of transmission.

SIG 4 LT to NT1

Signal which contains framing information and operational data on B and D channels.

SIG 5 NT1 to LT

Signal which contains framing information and operational data on B and D channels.

SIG 2-L2 LT to NT1

Signal similar to SIG 2, but includes a loopback 2 request.

SIG 4H-L2 LT to NT1

Signal which requires the NT1 to operate loopback 2 and to establish layer 1 information transfer capability in the direction LT to TE (transparent loopback 2).

SIG 4-L2

Signal similar to SIG 4, but includes a loopback 2 request.

All SIGs, except SIG 1W and SIG 2W, are continuous signals. The awake signals SIG 1W and SIG 2W are sent for a specified period of time only, but may be repeated if no acknowledgement is received. The repetition times are specified in a way to assure a proper interworking with the normal activation procedure.

The loopback requests are transmitted making use of the C_L channel. All other SIGs do not require the C_L channel.

The C_L channel shall be provided with all SIGs except SIG 0, SIG 1W, SIG 2W and SIG 1A.

B.10.2 Definition of internal timers

In the state transition tables and arrow diagrams the following internal timers are used:

- Tn1 = 13 ms: timer to supervise repetition of the awake signal SIG 2W from the LT;
- Tl1 = 7 ms: timer to supervise repetition of the awake signal SIG 1W from the NT1;
- Tl2 = 1 ms: timer which defines the duration of SIG 4H and SIG 4H-L2;
- Tl3 = 1 ms: timer which assures that, under non-failure conditions, the PH-AI shall be passed first in the TE and then in the LT/ET. This protects the first layer 2 frame (layer 3 - SETUP message) from the network side;
- Tl4 = 12 ms: timer used to start transmission of SIG 2 when loopback 1 is requested;
- Tl5 = 0,1... 1 s: timer to supervise the deactivation procedure (within ET).

NOTE: Existing realizations may reach the fully active state NT 1.7 before being able to detect a SIG 0 Deactivation Request. This can lead to a locking situation when a too fast deactivation and immediate subsequent activation are applied. To avoid this, the following measures are recommended to be applied by the ET:

- the activation shall last at least 1 s; or
- the start of the timer Tl 5 shall be delayed by 500 ms.

B.10.3 Description of the activation procedure

In figure B.2 the activation/deactivation procedures are described for the non-failure situation.

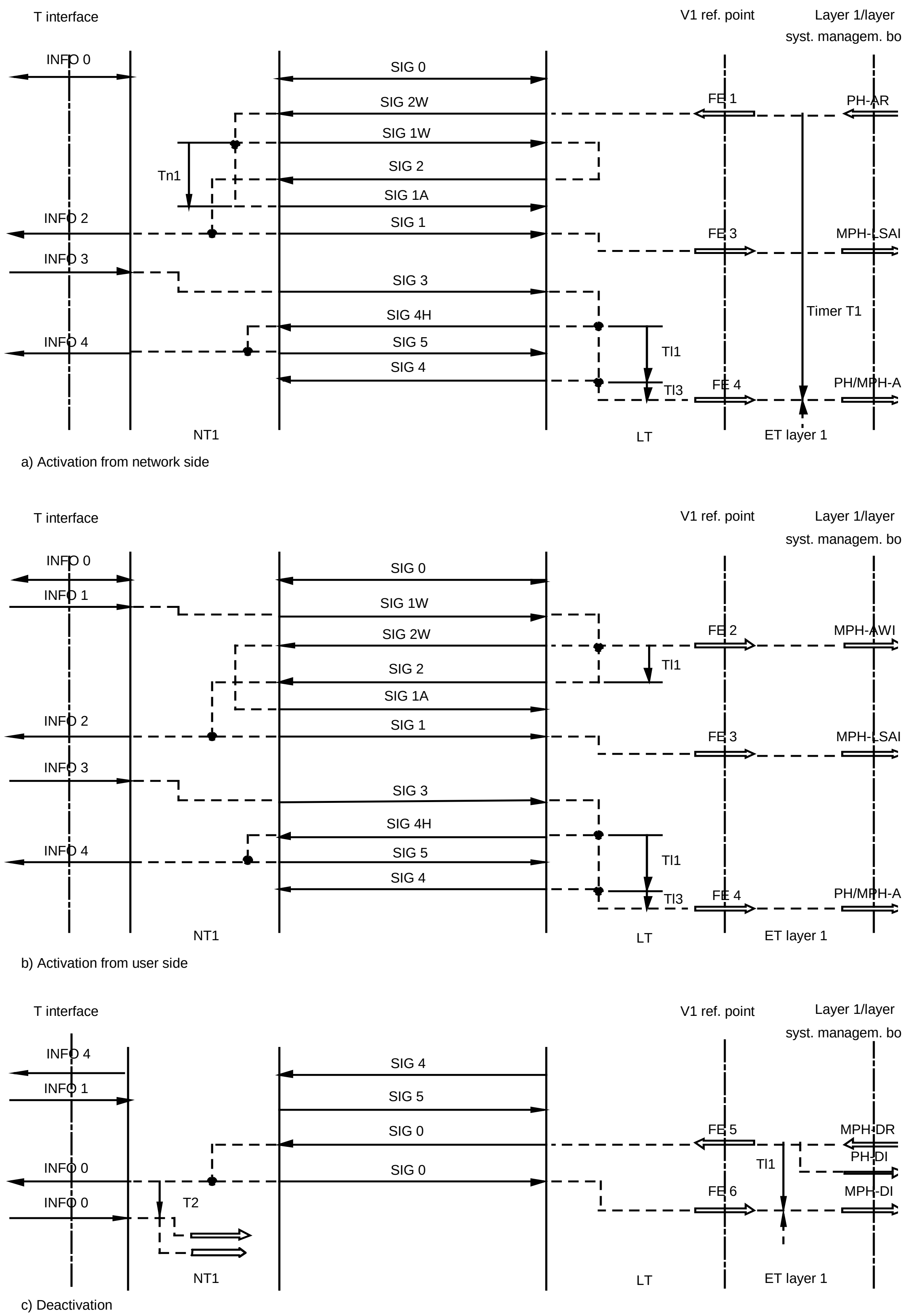


Figure B.2: Activation/deactivation procedures - arrow diagrams (non-failure situations)

Timer T1 (located in ET layer 1) and timer T2 (located in NT1) are as specified in ETS 300 012 [1]; the Function Elements (FEs) are defined in ETS 300 297 [4], subclause 8.4.3, and the primitives in ETS 300 297 [4], subclause A.3.2.

B.10.4 NT1 state transition table

The NT1 state transition table is described in table B.1. INFOs on the interface at T reference point are related to SIGs on the line system and vice versa.

Table B.1: NT1 state transition table

State	**NT1.1**	**NT1.2**	**NT1.3**	**NT1.4**	**NT1.5**	**NT1.6**	**NT1.7**	**NT1.8**	**NT1.9**	**NT1.10**	**NT2.1**	**NT2.2**
transmit signal	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 2**	**INFO 2**	**INFO 4**	**INFO 0**	**INFO 2**	**INFO X (note 2)**	**INFO 2**	**INFO 4 (note 4)**
receive signal	**SIG 0**	**SIG 1W**	**SIG 1W**	**SIG 1A**	**SIG 1**	**SIG 3**	**SIG 5**	**SIG 0**	**SIG 5**	**SIG 0 (note 3)**	**SIG 3**	**SIG 5 (note 5)**
INFO 0	-	-	-	-	-	-	NT 1.9	NT 1.1	-	-	-	-
INFO 1	NT 1.2	-	-	-	-	-	/	-	-	/	-	/
INFO 3	/	/	/	/	NT 1.6	-	-	-	NT 1.7	/	-	-
SIG 0	-	-	-	ST.T2; NT 1.8	ST.T2; NT 1.8	ST.T2; NT 1.8	ST.T2; NT 1.8	-	ST.T2; NT 1.8	ST.T2; NT 1.8	ST.T2; NT 1.8	ST.T2; NT 1.8
SIG 2W	ST.Tn1; NT 1.3	NT 1.4	/	/	/	/	/	-	/	/	/	/
SIG 2	/	-	-	NT 1.5	-	-	/	/	/	/	NT 1.6 or -	/
SIG 4H	/	/	/	/	/	NT 1.7	-	/	/	/	NT 1.7	/
SIG 4	/	/	/	/	/	/	-	/	-	-	/	NT 1.7
Exp. T2 (note 1)	-	-	-	-	-	-	-	NT 1.1	-	-	-	-
Lost framing T interface	/	/	/	/	/	-	NT 1.9	-	-	-	/	/
Lost framing line system	/	/	/	/	NT 1.10	NT 1.10	NT 1.10	/	NT 1.10	-	NT 1.10	NT 1.10
Exp. of internal timer Tn1	/	/	NT 1.4	/	/	/	/	/	/	/	/	/
SIG 2-L2	/	-	-	NT 2.1	NT 2.1 or -	NT 2.1 or -	/	/	/	/	-	/
SIG 4H-L2	/	/	/	/	/	NT 2.2	-	/	/	/	NT 2.2	-
SIG 4-L2	/	/	/	/	/	/	NT 2.2	/	NT 2.2	NT 2.2	/	-

- No state change.
/ Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons.

ST.Tnx; NTy: Start timer x; enter state NT y.

NOTE 1: Timer T2 as defined in ETS 300 012 [1].
NOTE 2: INFO X: signal with no framing information i.e. binary ZEROs.
NOTE 3: Any other signal which produces an error indication on the LT side is allowed, especially loss of framing or excessive error rate.
NOTE 4: The D-Echo bit is set to binary ZERO.
NOTE 5: The B- and D-channels are looped back to the network side.

The following states are used:

- NT 1.1 - Deactivated state (low power consumption mode). No signal shall be transmitted;

- NT 1.2 - The NT1 sends the awake signal SIG 1W to the LT, on the receipt of INFO 1 from the user side, and waits for the receipt of the awake acknowledge signal SIG 2W from the LT;

- NT 1.3 - On receipt of the awake signal SIG 2W, the NT1 responds with SIG 1W and starts transmission of SIG 1A on expiry of timer Tn1, unless a new awake signal SIG 2W from the LT is received;

- NT 1.4 - After completion of the awake procedure, the NT1 waits for SIG 2 to synchronize its receiver;

- NT 1.5 - The receiver on the network side shall be synchronized. The NT1 sends SIG 1 to the LT and INFO 2 to the user side to initiate the activation of the interface at reference point T. It waits for the receipt of INFO 3;
- NT 1.6 - The interface at T reference point shall be synchronized in both directions of transmission. The NT1 sends;
- NT 1.7 - The NT1 shall be fully active and sends INFO 4 to the user side and SIG 5 to the LT. The B-channels and D-channels are operational;
- NT 1.8 - Pending deactivation state. The NT1 sends INFO 0 to the user side to deactivate the interface at reference point T and SIG 0 to the LT. It waits for the receipt of INFO 0 or expiry of timer T2 to enter state NT1.1;
- NT 1.9 - This state shall be entered on loss of signal or loss of framing at the interface at T reference point. No indication shall be sent to the LT;
- NT 1.10 - This state shall be entered on loss of framing at the line side. An indication shall be forwarded to the user side (INFO X) and to the network side (SIG 0).

The following states support activation when loopback 2 is requested:

- NT 2.1 - The receiver on the network side shall be synchronized. The NT1 sends SIG 3 to the LT and INFO 2 to the user side (transparent loopback). It waits for the receipt of SIG 4H-L2 from the LT;
- NT 2.2 - The NT1 is fully active and sends INFO 4 to the user side (transparent loopback) and SIG 5 to the LT. Loopback 2 is operated and receive data 2B+D are sent to the LT.

B.10.5 LT state transition table

The LT state transition table is described in table B.2. SIGs on the line system are related to FEs on the V1 reference point.

Table B.2: LT state transition table

State	LT 1.1	LT 1.2	LT 1.3	LT 1.4	LT 1.5	LT 1.6	LT 1.7	LT 1.8	LT 2.1	LT 2.2	LT 2.3	LT 2.4
transmit signal receive signal	**SIG 0**	**SIG 2W**	**SIG 2W**	**SIG 2**	**SIG 2**	**SIG 4H**	**SIG 4**	**SIG 0**	**SIG 2W**	**SIG 2**	**SIG 4H**	**SIG 4**
FE 1	LT 1.3	-	-	-	-	-	-	-	-	-	-	-
FE 5	:	LT 1.8	LT 1.8	LT 1.8	LT 1.8	LT 1.8	LT 1.8	-	LT 1.8	LT 1.8	LT 1.8	LT 1.8
SIG 0	-	-	-	-	FE 7;	FE 7;	FE 7;	FE 6; LT 1.1	-	-	-	-
SIG 1W	ST.TI 1 FE 2; LT 1.2	:	LT 1.4	/	/	/	/	-	-	/	/	/
SIG 1	/	/	/	FE 3; LT 1.5	-	/	/	-	/	-	-	-
SIG 3	/	/	/	ST.TI 2LT 1.6;	ST.TI 2LT 1.6;	-	-	-	/	-	-	-
Exp. of internal timer TI1	-	LT 1.4	-	-	-	-	-	-	-	-	-	-
Exp. of internal timer TI2	-	-	-	-	-	FE 7; LT 1.4	-	-	-	-	FE 4; LT 2.4	-
Lost framing line system	/	/	/	/	FE 7;	FE 7:	FE 7;	-	/	/	/	/
FE 4	ST.TI 4; LT 2.1	-	LT 2.2 or -	LT 2.2 or -	LT 2.2 or -	-	-	LT 2.1	:	:	:	:
Exp. of internal timer TI4	-	-	-	-	-	-	-	-	LT 2.2	-	-	-
Rec. synch. on looped back sig.	/	/	/	-	-	-	-	-	/	ST.TI 2; LT 2.3	-	-

-	No state change.
/	Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons.
:	Impossible by the definition of the physical layer.
a, b;	LTx Perform action/issue message a and b; enter state LTx.
ST.Tlx	Start timer Tlx.

The following states are used:

- LT 1.1 - Deactivated state. No signal shall be transmitted;
- LT.1.2 - On receipt of the awake signal SIG 1W, the LT responds with SIG 2W and starts transmission of SIG 2 on expiry of timer Tl1, unless a new awake signal SIG 1W from the NT1 is received;
- LT.1.3 - The LT sends the awake signal SIG 2W to the NT1, on the receipt of FE 1, and waits for the awake acknowledge signal SIG 1W from the NT1;
- LT.1.4 - The LT sends SIG 2 to the NT1 and waits for SIG 1 or SIG 3 to synchronize its receiver. When the LT is synchronized and has detected SIG 1, it issues FE 3;
- LT.1.5 - The line transmission system shall be synchronized in both directions of transmission. The LT waits for the receipt of SIG 3;
- LT.1.6 - The line transmission system and the interface at T reference point are synchronized in both directions of transmission. The LT sends SIG 4H until the expiry of timer Tl2;

- LT.1.7 - Fully active state. The LT sends SIG 4 to the NT1 and issues FE 4. The B-channels and D-channel are fully operational;
- LT.1.8 - Pending deactivation state. The LT sends SIG 0 to the NT1 to deactivate the line system and the interface at T reference point. It waits for the receipt of SIG 0 to enter state LT 1.1 and to issue FE 6.

The following states support activation when loopback 1 is requested:

- LT.2.1 - The LT sends the awake signal SIG 2W to the NT1 (transparent loopback), on the receipt of FE 9, and starts transmission of SIG 2 on expiry of timer Tl4;
- LT.2.2 - The LT has operated loopback 1 and is synchronizing its receiver on the looped back signal;
- LT.2.3 - The LT sends SIG 4H until the expiry of timer Tl2;
- LT.2.4 - The LT is fully active and sends SIG 4 to the NT1 (transparent loopback). Loopback 1 is operated.

The LT state transition table shall not be affected by loopback 2 and 1A requests. The corresponding control signals are transferred across channels C_{V1} and C_L.

B.10.6 Activation times

For definition of activation times see ETS 300 297 [4], subclause 8.5:

a) maximum activation time for activation occurring immediately after a deactivation:

- without regenerator: 210 ms;
- with regenerator: 420 ms.

b) maximum time for activation occurring after the first powering of a line:

- without regenerator: 1,5 s;
- with regenerator: 3 s.

B.11 Jitter

Jitter tolerances shall assure that the maximum network limit of jitter (see ITU-T Recommendation G.823 [11]) is not exceeded. Furthermore, the limits of ETS 300 012 [1] shall be supported by the jitter limits of the transmission system on local lines.

The jitter limits given below shall be satisfied regardless of the length of the local line and the inclusion of repeaters, provided that they are covered by the transmission media characteristic (see clause 3). The limits shall be met regardless of the transmitted signal. A suitable test sequence is for further study (see ITU-T Recommendation G.823 [11], § 4).

B.11.1 Limits of maximum tolerable input jitter

The amplitude of the jitter at the NT1 input shall be limited by the template given in figure B.3.

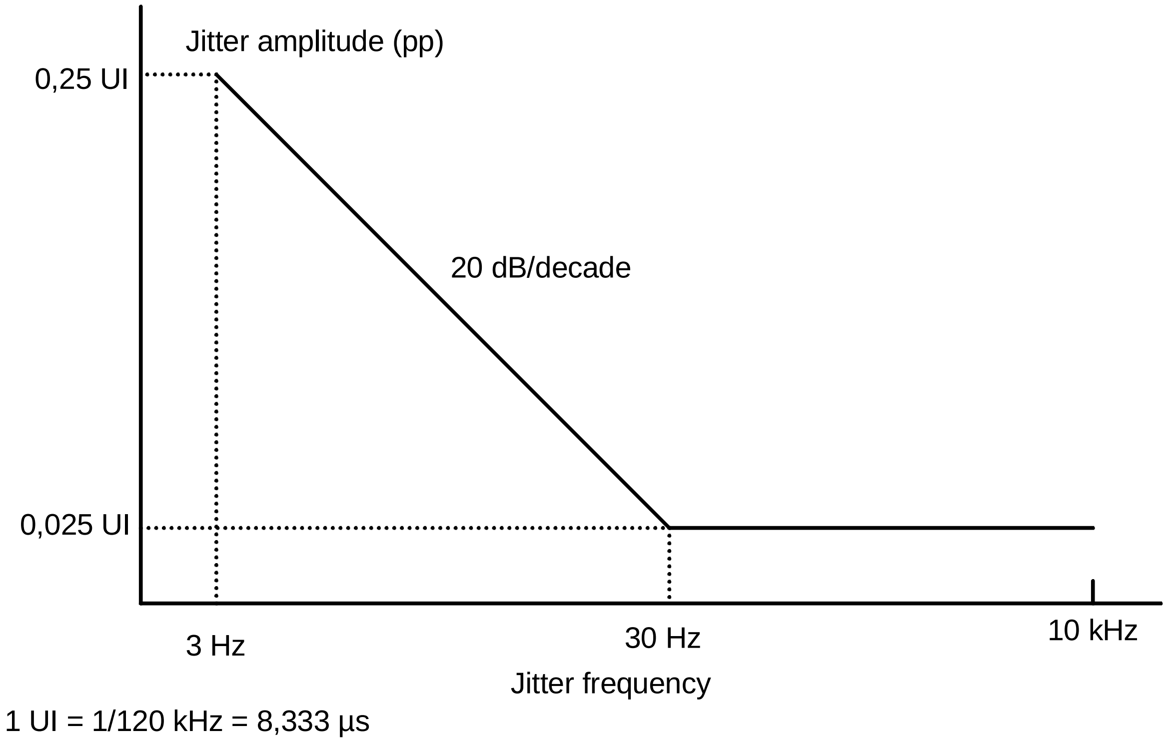


Figure B.3: Maximum tolerable sinusoidal input jitter

B.11.2 Output jitter of NT1 in absence of input jitter

When measured with a highpass filter with a 30 Hz cut-off frequency, the jitter at the output of the NT1 shall not exceed 0,02 UIpp. Without a filter, the jitter shall not exceed 0,1 UIpp.

B.11.3 Timing extraction jitter

The jitter at the output of the NT1 shall closely follow the input jitter. Therefore, the jitter transfer function of the NT1 shall be less than ± 1 dB in the frequency range 3 Hz to 30 Hz.

B.11.4 Test conditions for jitter measurements

For further study.

B.12 Transmitter output characteristics

B.12.1 Pulse amplitude

The amplitude of a transmitted single pulse shall be 2 V ± 0,2 V with a load impedance of 150 Ω.

B.12.2 Pulse shape

The shape of a transmitted single pulse shall fit the mask given in figure B.4.

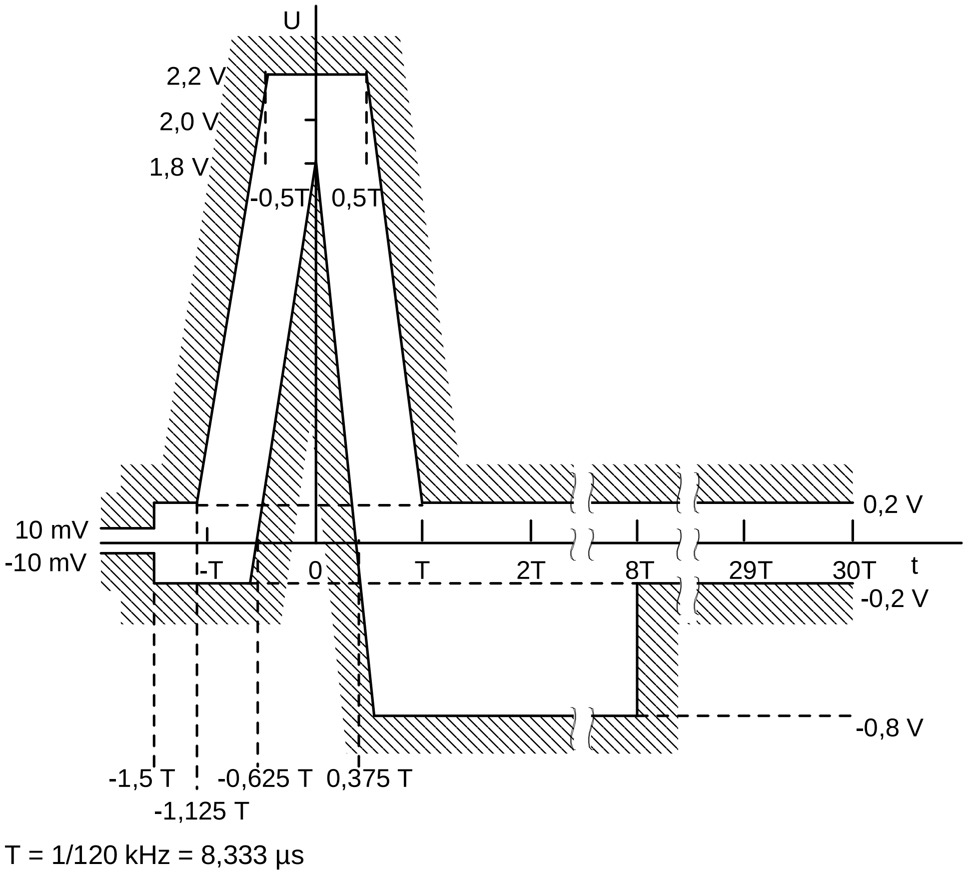


Figure B.4: Pulse mask for transmitted single pulse

B.12.3 Signal power

Not specified.

B.12.4 Power spectral density

The upper bound of the power spectral density shall be limited according to figure B.5. Measurements to verify compliance with this requirement are to use a bandwidth of 10 kHz.

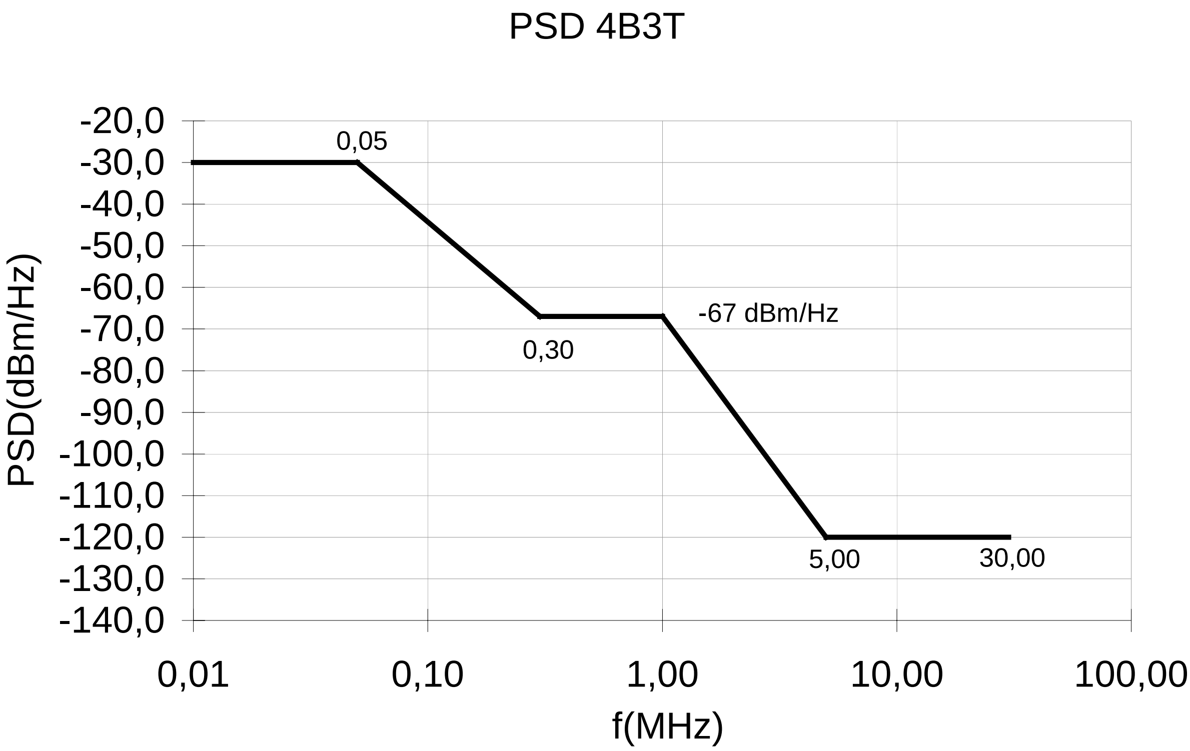


Figure B.5: Upper bound of power spectral density from NT1 and LT

Systems deployed before January 1, 2000, do not have to meet this PSD requirement but shall meet the PSD requirements as defined in ETR 080 [17]. It is however expected that these systems will also meet the PSD requirements of the present document although some narrow-band violations could occur and should be tolerated.

B.12.4.1 Sliding window PSD requirement

The purpose of the sliding window is to perform a higher bandwidth measurement in order to make sure that different systems do not fill the entire allowable band with noise up to the limit shown in figure B.12 300 kHz. The sliding window parameters and values are given in table B.3.

Table B.3: Sliding window parameters and values

PARAMETER	VALUE
Bandwidth of sliding window	1 MHz
Reference frequency	Lower edge
Step size	10 kHz
Start frequency	300 kHz
Stop frequency	29 MHz

The sliding window PSD shall be measured as the total average power within a 1 MHz sliding window (1MHz bandwidth). The result shall be less -120 dBm/Hz or at least more than 7 dB below the PSD limit shown in figure B.5. The requirement is applicable between 300 kHz and 30 MHz.

Systems deployed before January 1. 2000, do not have to meet the sliding window PSD requirement.

B.12.5 Transmitter signal non-linearity

Not specified.

B.13 Transmitter/receiver termination

B.13.1 Impedance

The nominal output/input impedance of the NT1 and LT shall be 150 Ω.

B.13.2 Return loss

The return loss against 150 Ω ± 1 % measured for NT1 or LT shall exceed the limits given in figure B.6.

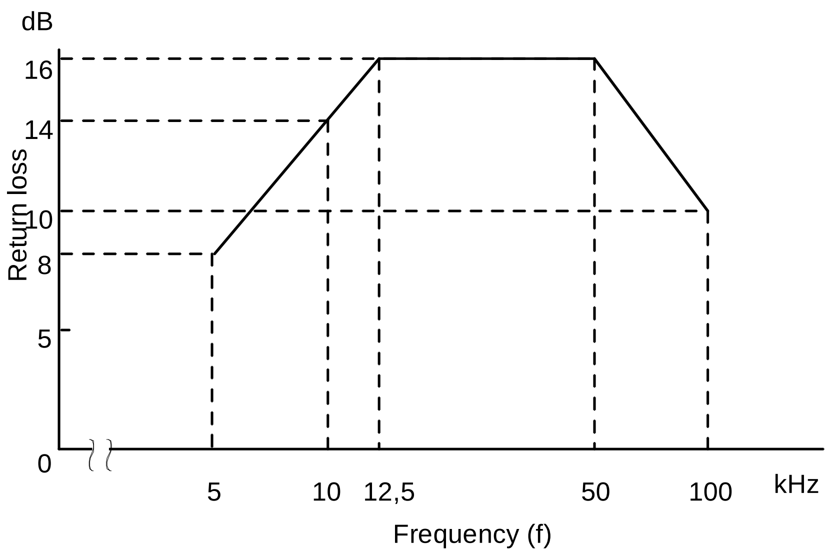


Figure B.6: Minimum NT1 and LT return loss

B.13.3 Longitudinal conversion loss

The longitudinal conversion loss at the line interface for LT and NT1 shall exceed the limits given in figure B.7.

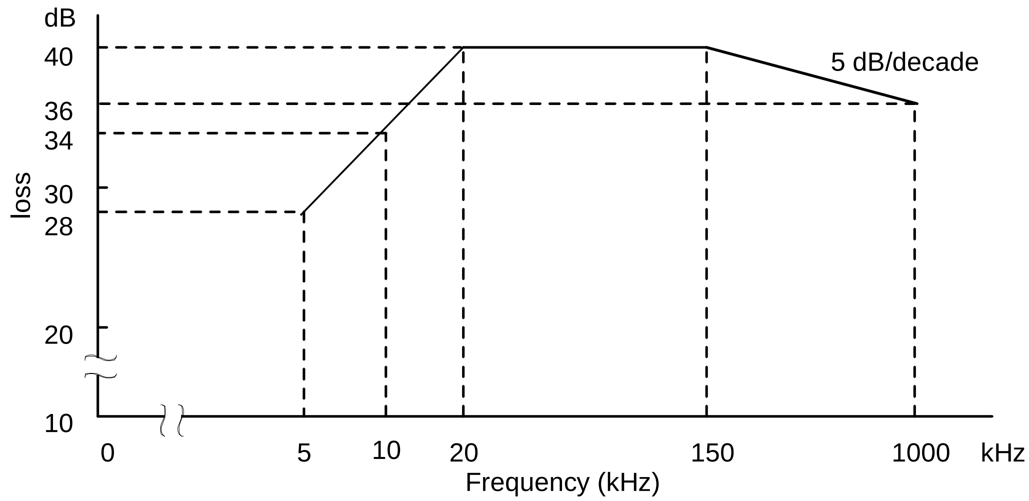


Figure B.7: Minimum longitudinal conversion loss

Annex B1 (informative): Extension functions for a system with MMS43 line code

No extension functions and requirements have been defined yet.

Annex C (informative): Detailed test cable characteristics

C.1 Parameters for test cables

C.1.1 Parameters of 0,4 mm PE cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	268	269	271	282	312	390
L' (μH/km)	678	675	669	650	635	619
C' (nF/km)	45,5	45,5	45,5	45,5	45,5	45,5

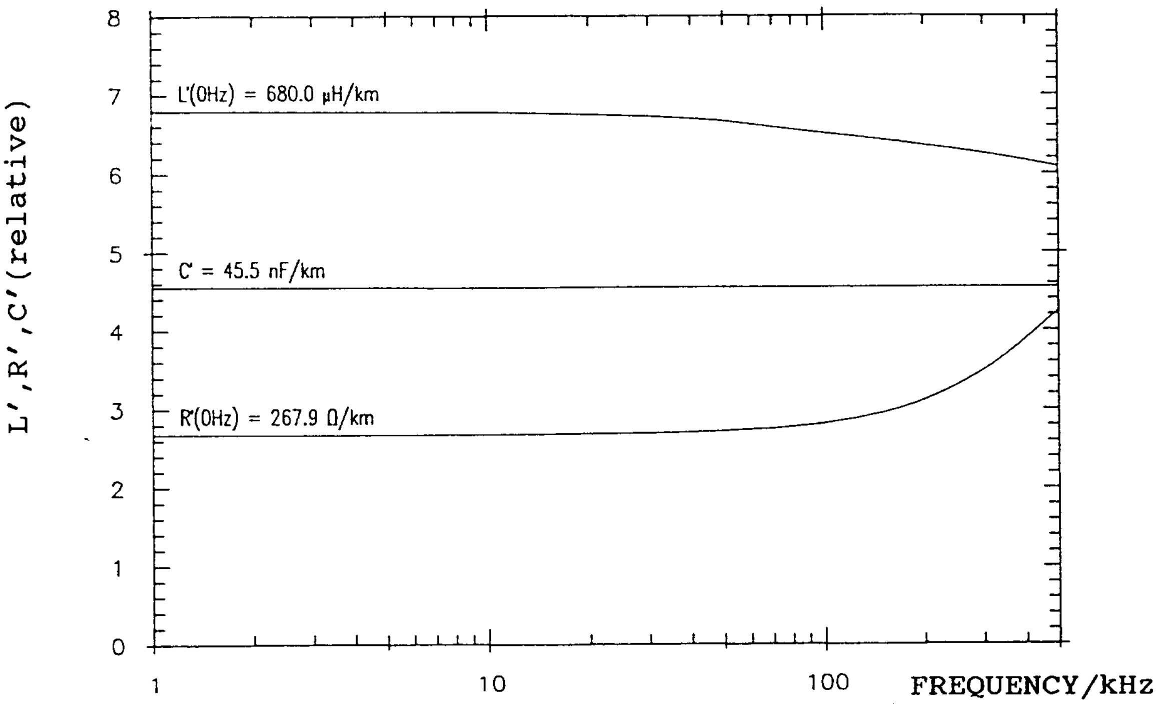


Figure C.1: Parameters of 0,4 mm PE cable

C.1.2 Parameters of 0,5 mm PE cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	172	173	175	190	227	302
L' (µH/km)	678	675	667	646	629	603
C' (nF/km)	25	25	25	25	25	25

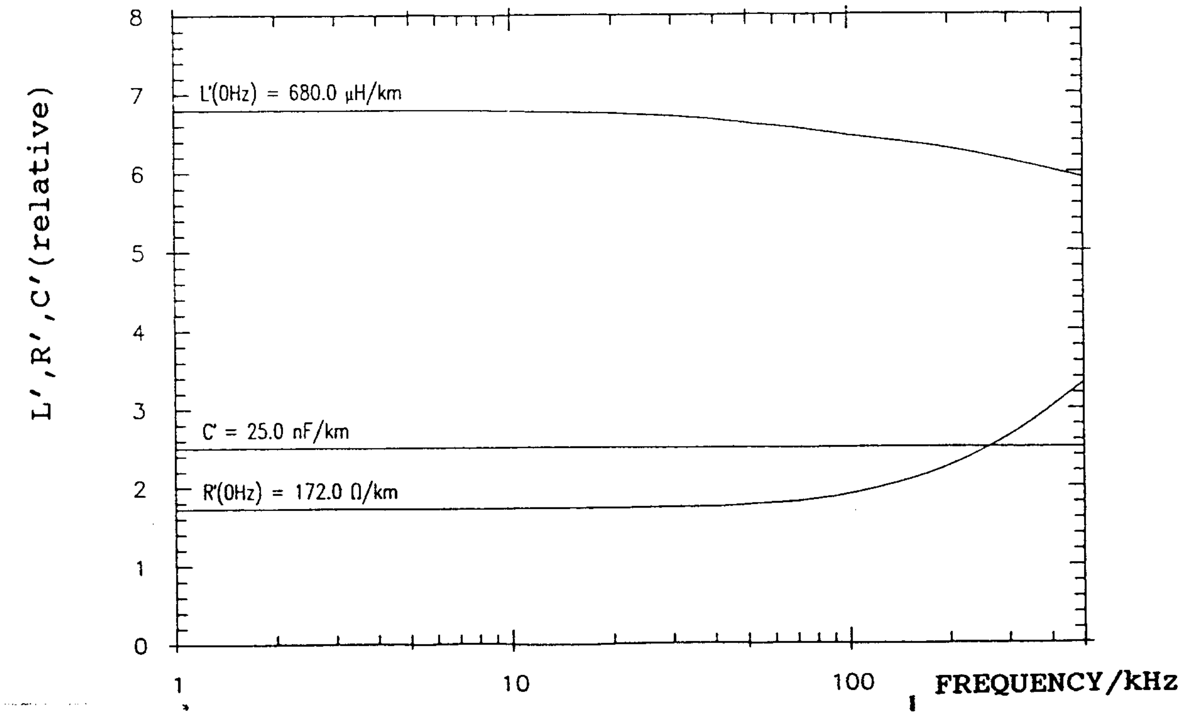


Figure C.2: Parameters of 0,5 mm PE cable

C.1.3 Parameters of 0,6 mm PE cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	120	121	125	146	189	260
L' (μH/km)	695	693	680	655	633	601
C' (nF/km)	56	56	56	56	56	56

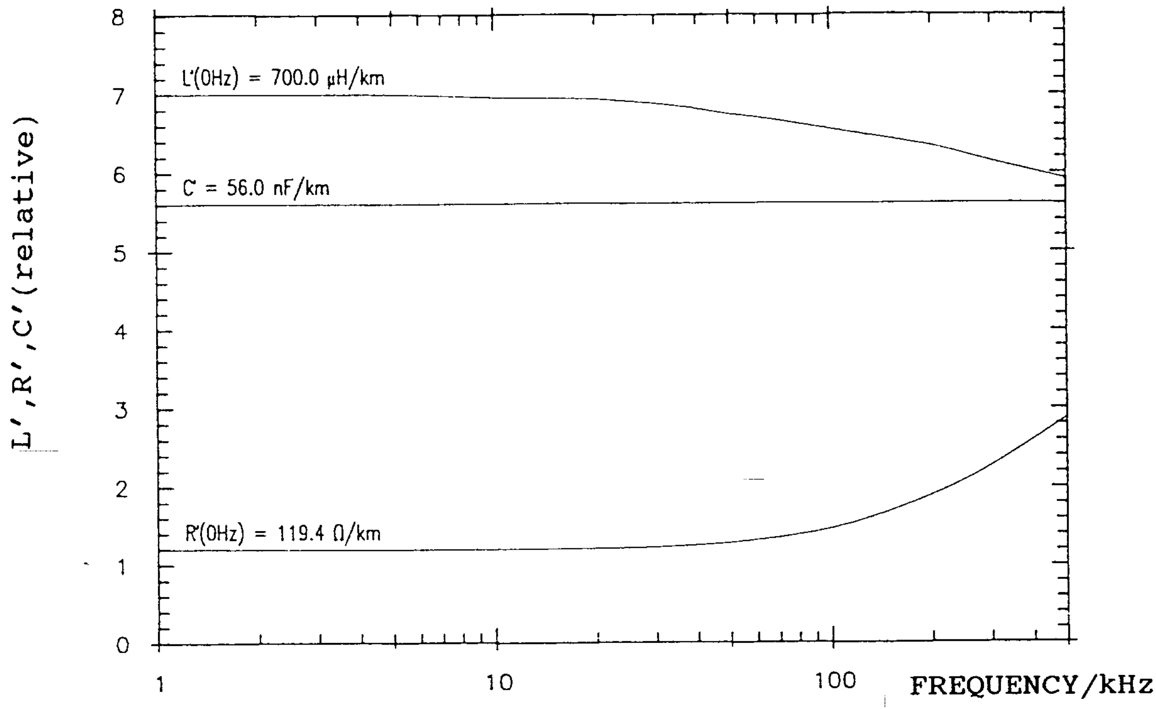


Figure C.3: Parameters of 0,6 mm PE cable

C.1.4 Parameters of 0,8 mm PE cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	80,0	72,5	75,0	91,7	117	159
L' (μH/km)	700	687	665	628	595	558
C' (nF/km)	37,8	37,8	37,8	37,8	37,8	37,8

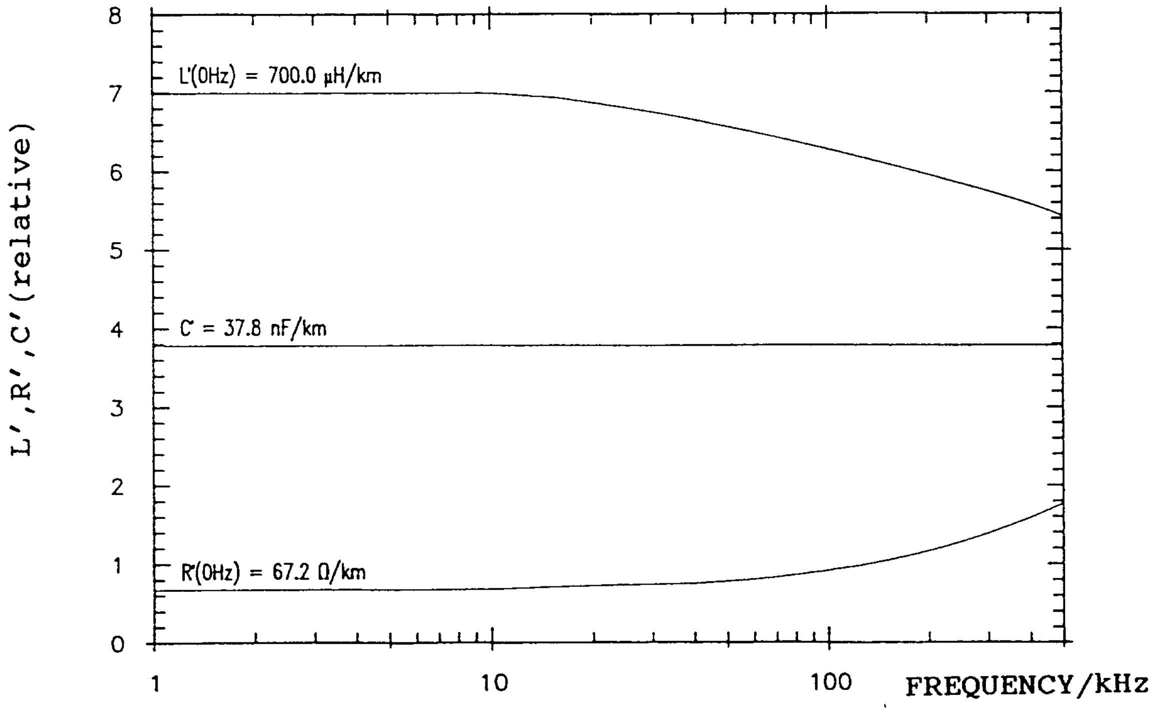


Figure C.4: Parameters of 0,8 mm PE cable

C.1.5 Parameters of 0,32 mm PVC cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	419	419	419	427	493	679
L' (μH/km)	650	650	650	647	621	577
C' (nF/km)	120	120	120	120	120	120

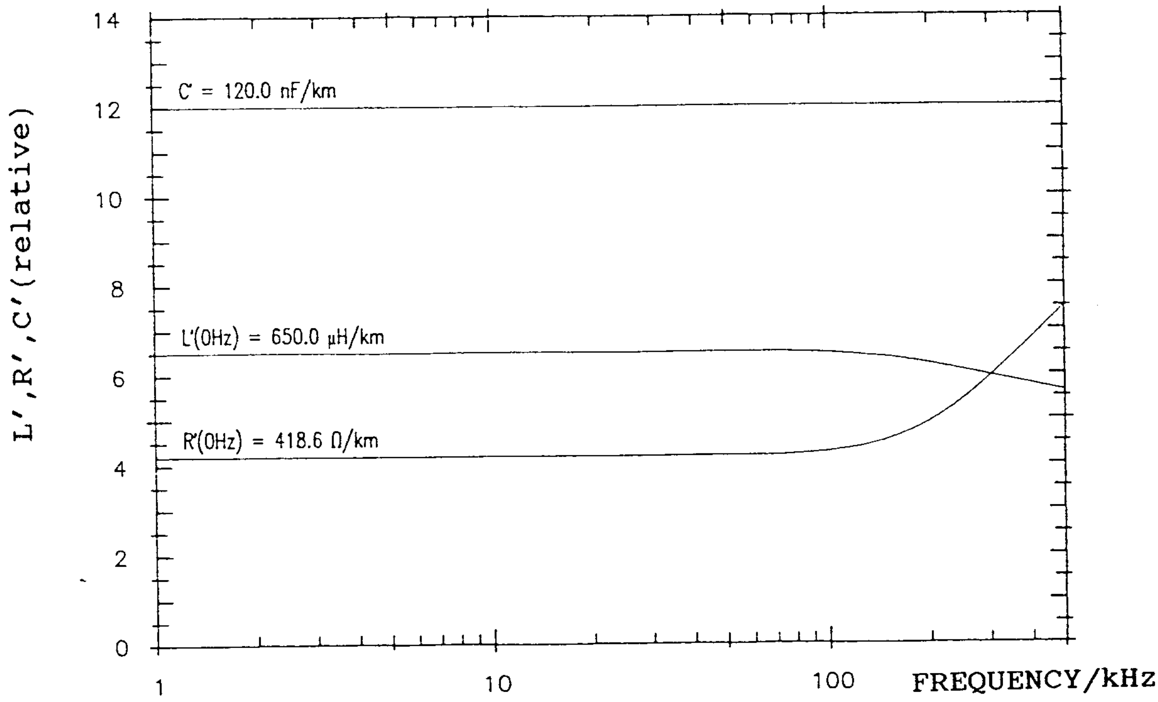


Figure C.5: Parameters of 0,32 mm PVC cable

C.1.6 Parameters of 0,4 mm PVC cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	268	268	268	281	311	391
L' (µH/km)	650	650	650	635	619	592
C' (nF/km)	120	120	120	120	120	120

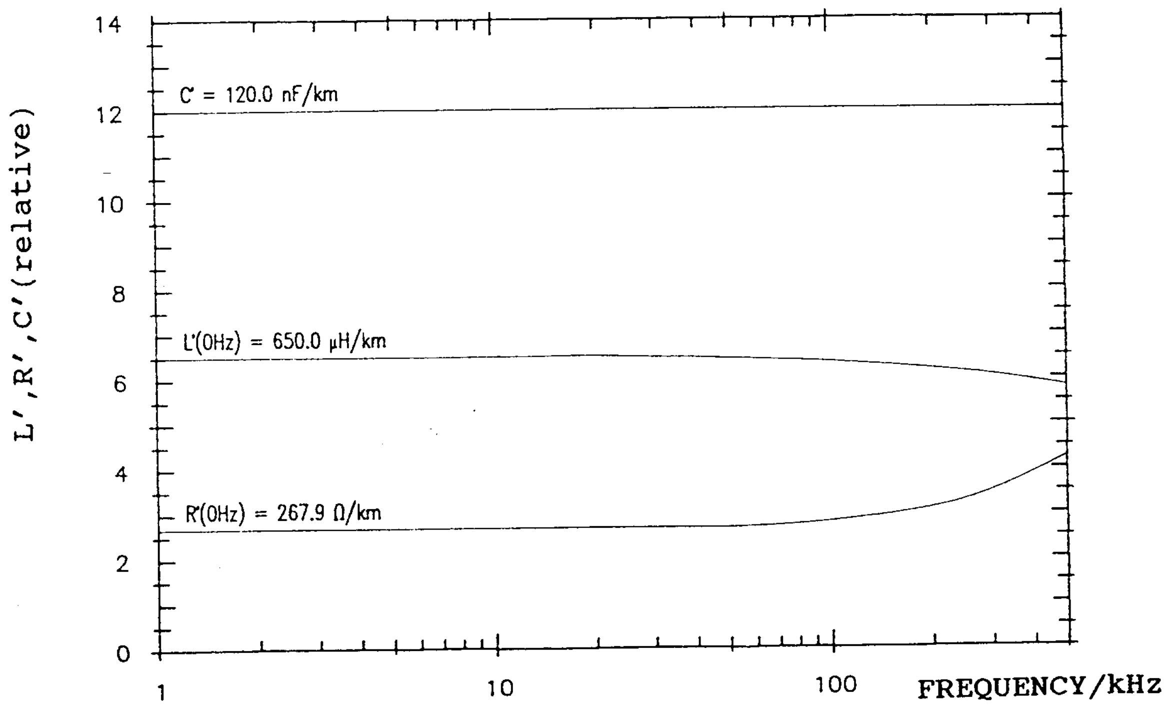


Figure C.6: Parameters of 0,4 mm PVC cable

C.1.7 Parameters of 0,63 mm PVC cable

Frequency (kHz)	10	20	40	100	200	400
R' (Ω/km)	108	108	111	141	207	319
L' (µH/km)	635	635	630	604	560	492
C' (nF/km)	120	120	120	120	120	120

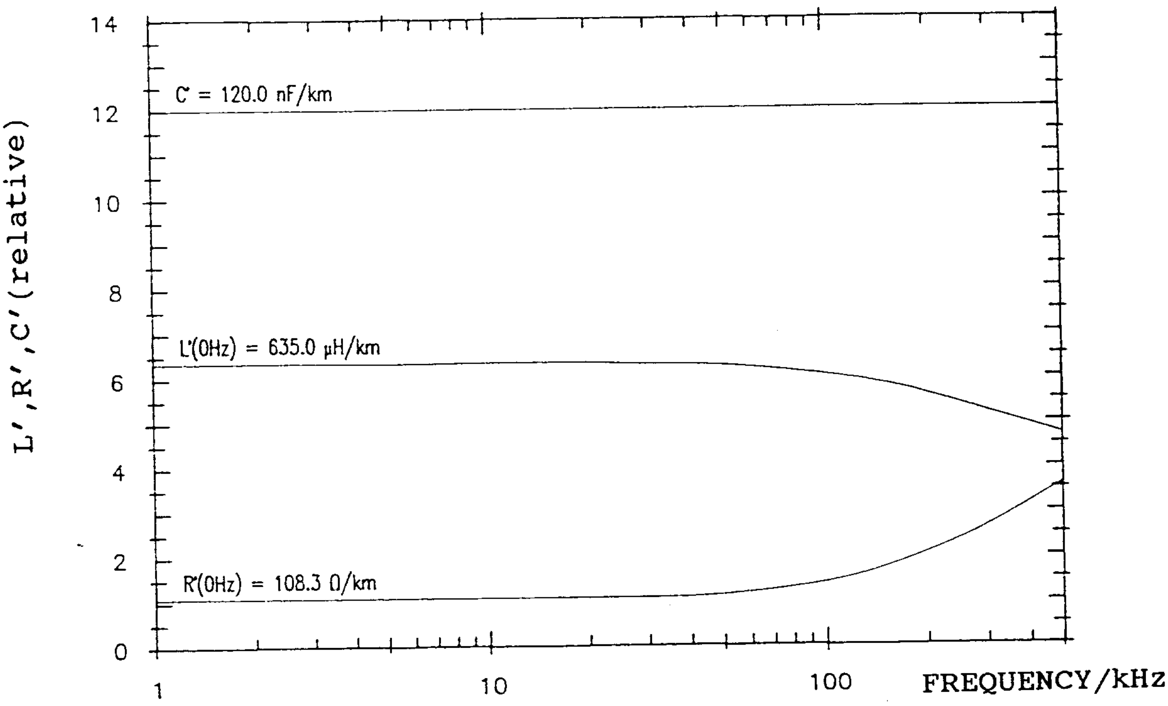


Figure C.7: Parameters of 0,63 mm PVC cable

C.2 Impedance plot of test loops

C.2.1 Impedance plot at 10 kHz

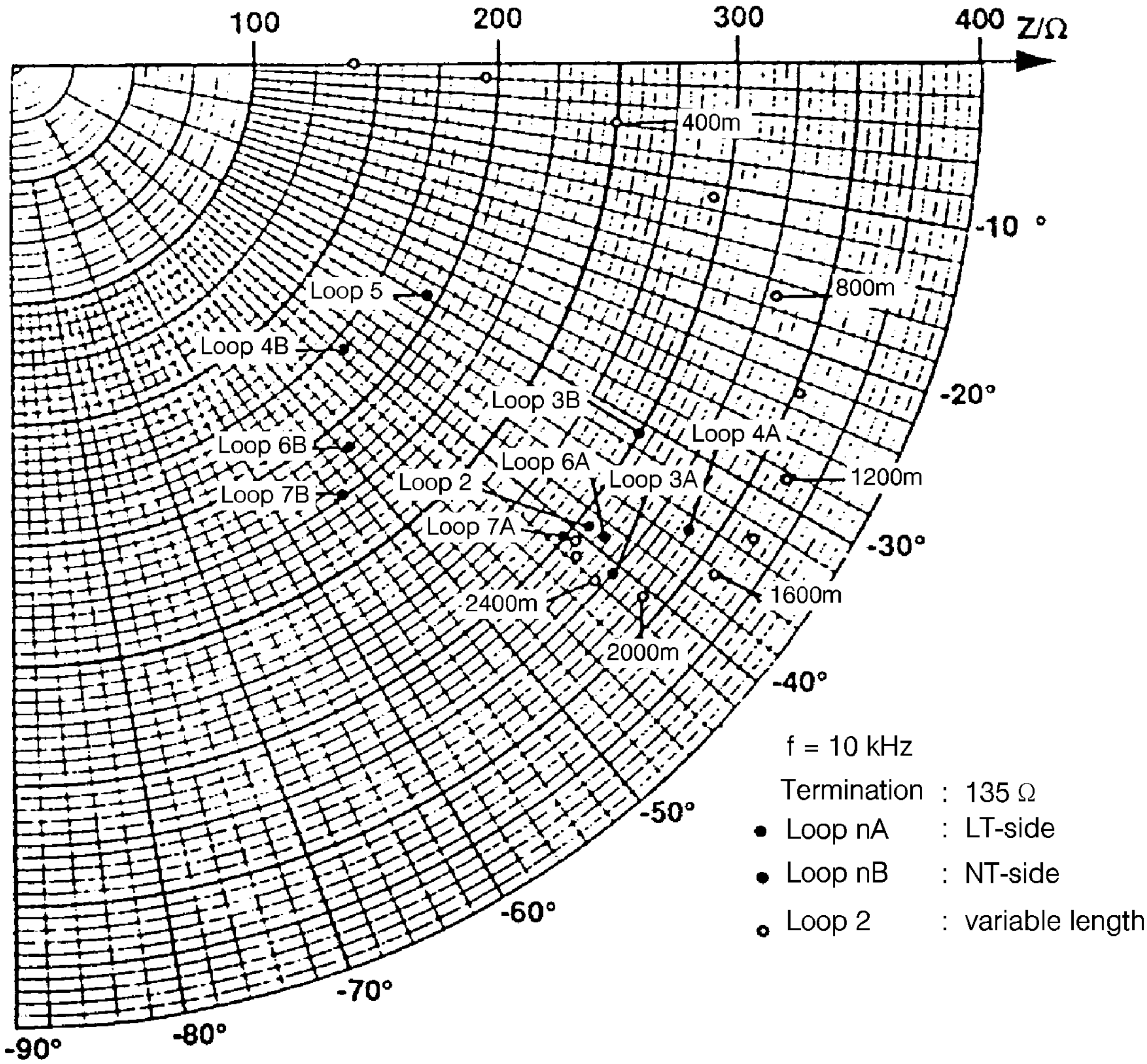


Figure C.8: Impedance plot at 10 kHz

C.2.2 Impedance plot at 20 kHz

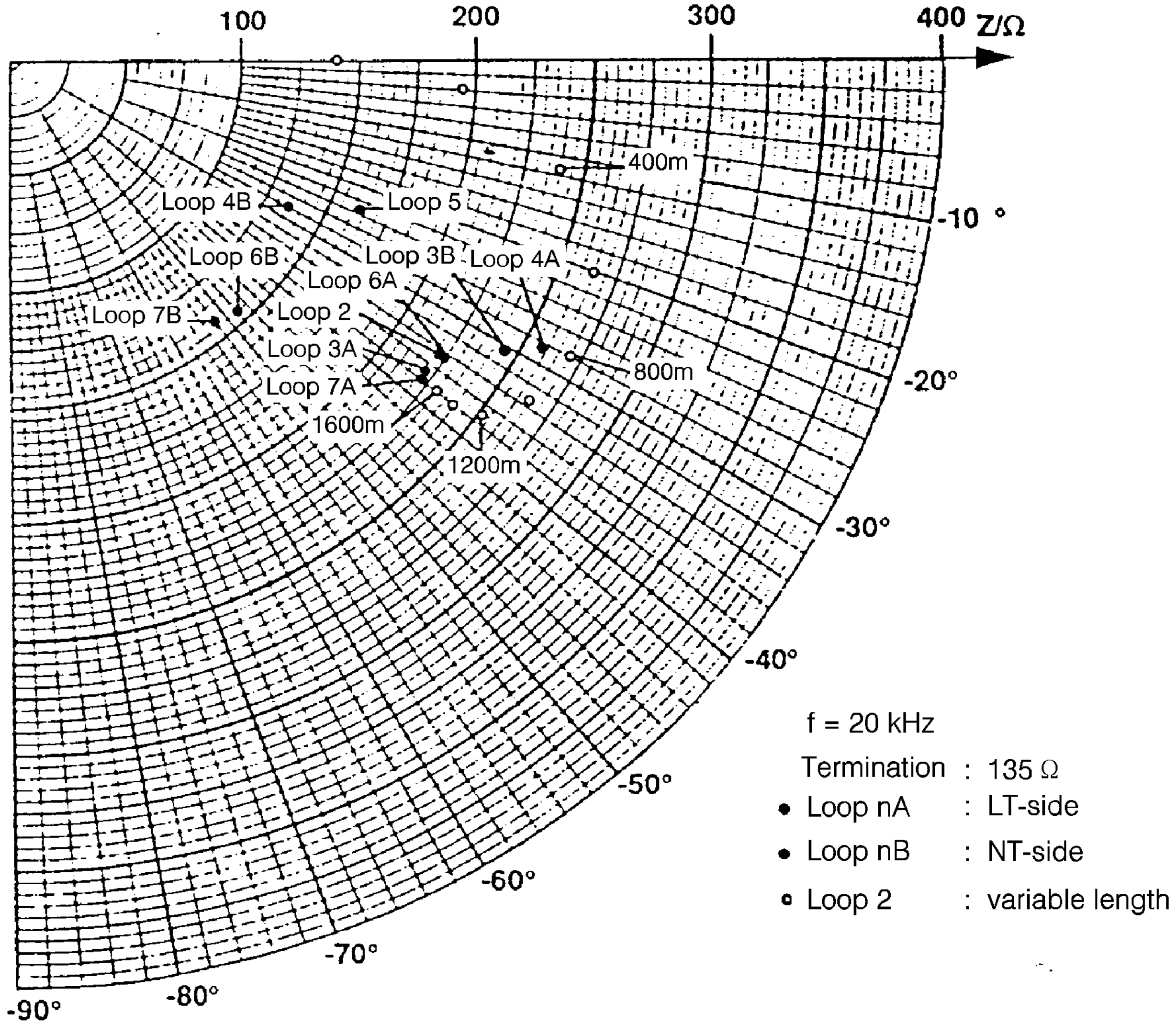


Figure C.9: Impedance plot at 20 kHz

C.2.3 Impedance plot at 40 kHz

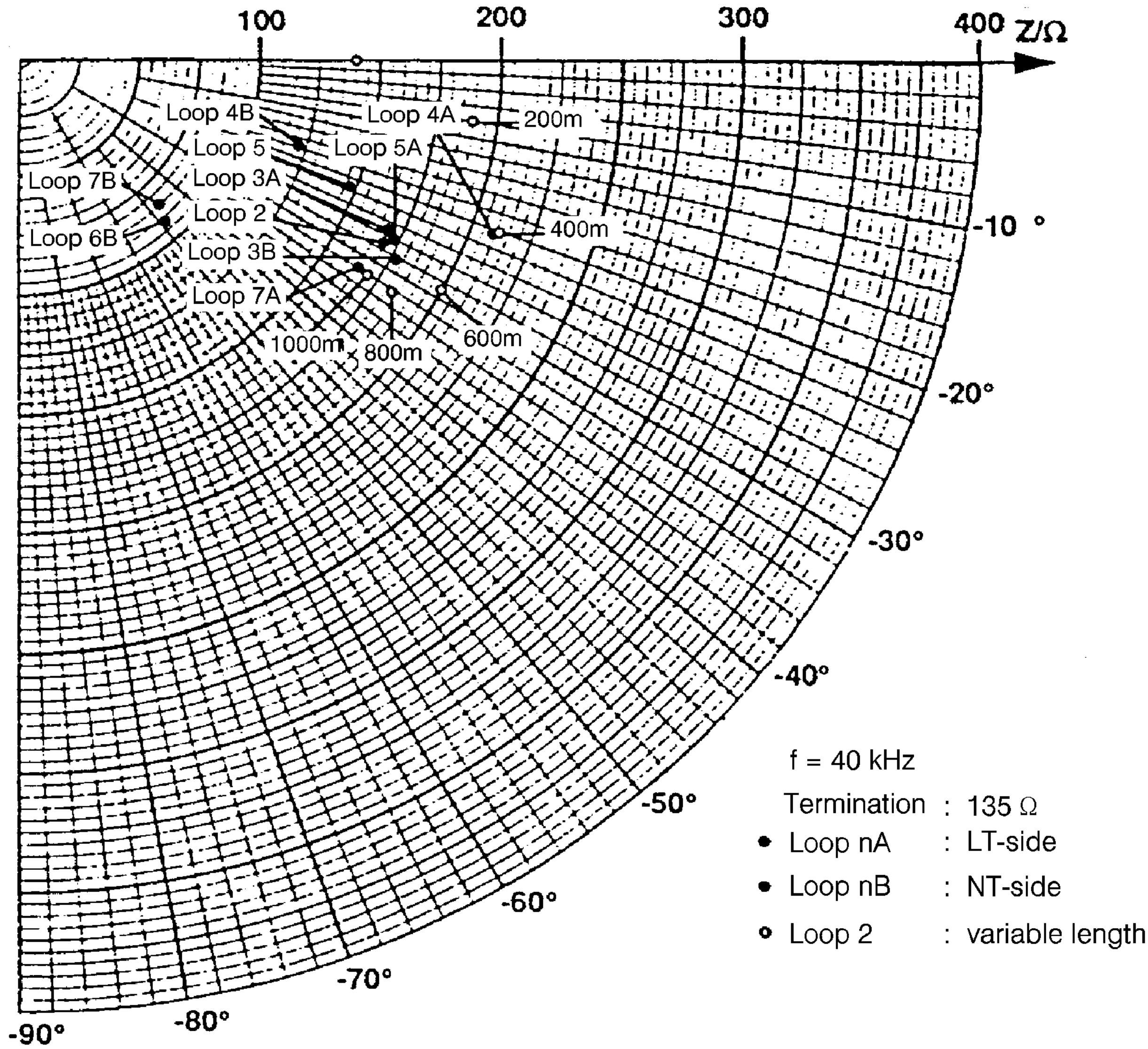


Figure C.10: Impedance plot at 40 kHz

C.2.4 Impedance plot loop 9

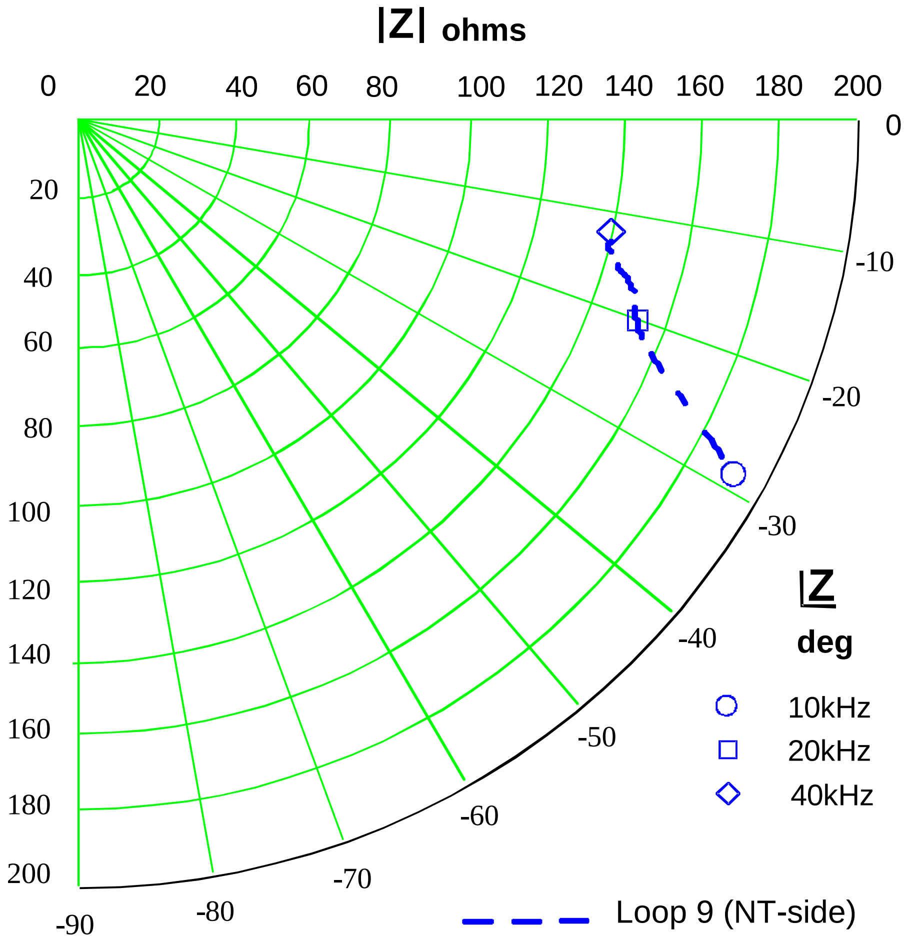


Figure C.11: Impedance plot loop 9 NT-side

C.3 Frequency response of test loops

C.3.1 Frequency response of loop 2

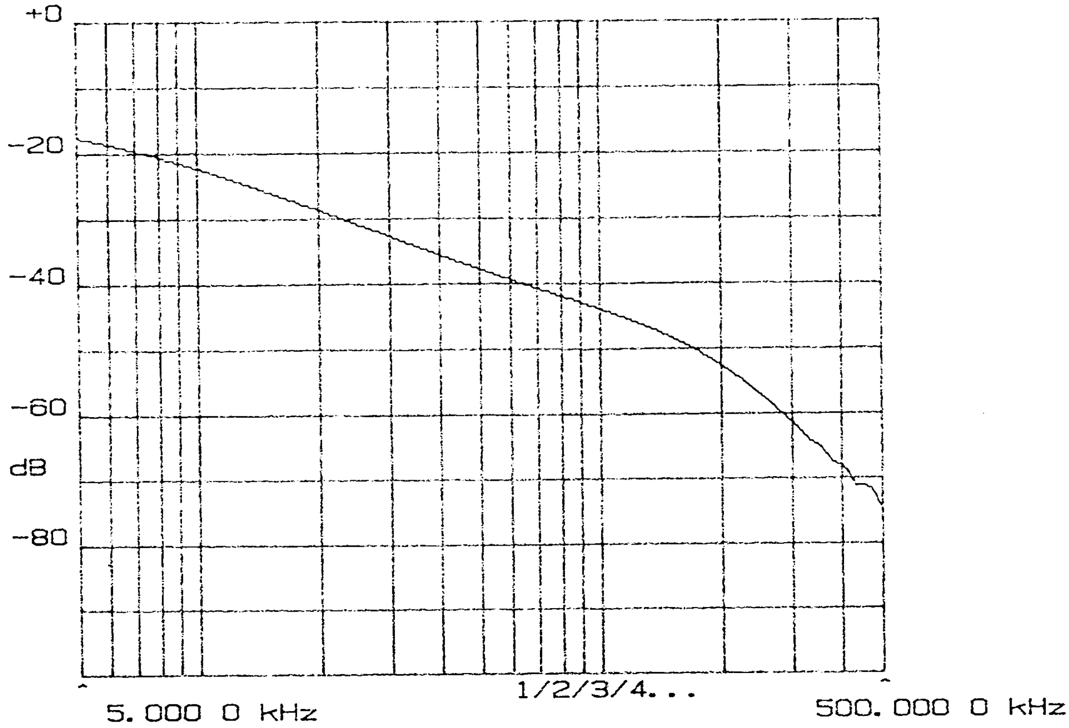


Figure C.11A: Frequency response of loop 2

C.3.2 Frequency response of loop 3

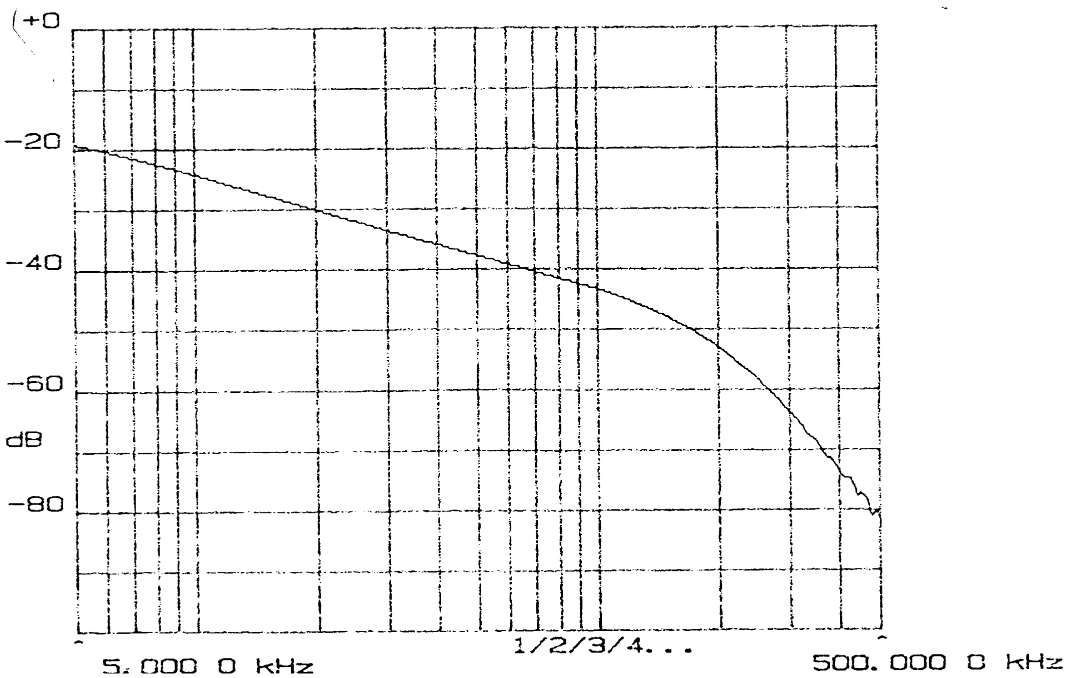


Figure C.12: Frequency response of loop 3

C.3.3 Frequency response of loop 4

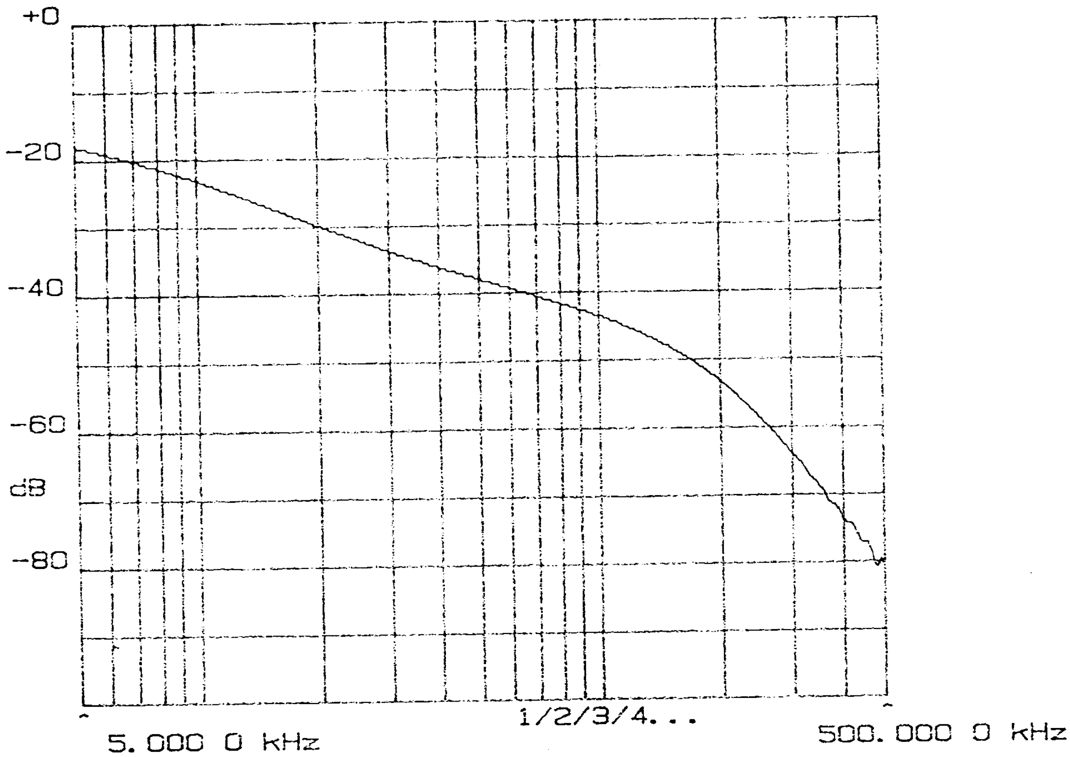


Figure C.13: Frequency response of loop 4

C.3.4 Frequency response of loop 5

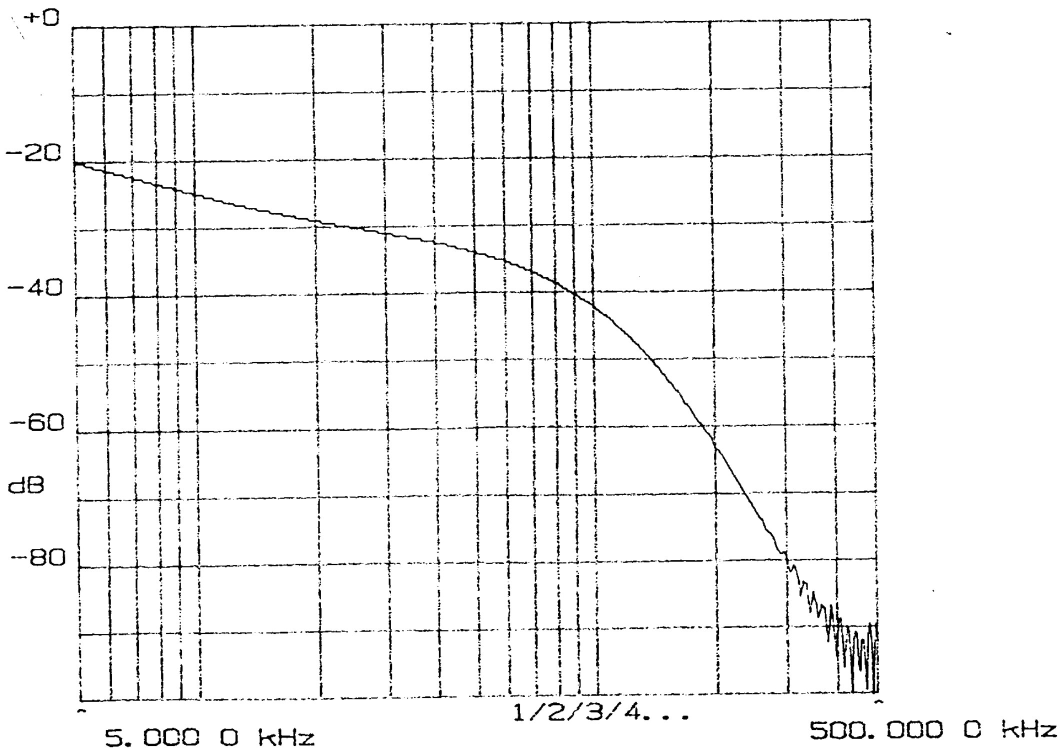


Figure C.14: Frequency response of loop 5

C.3.5 Frequency response of loop 6

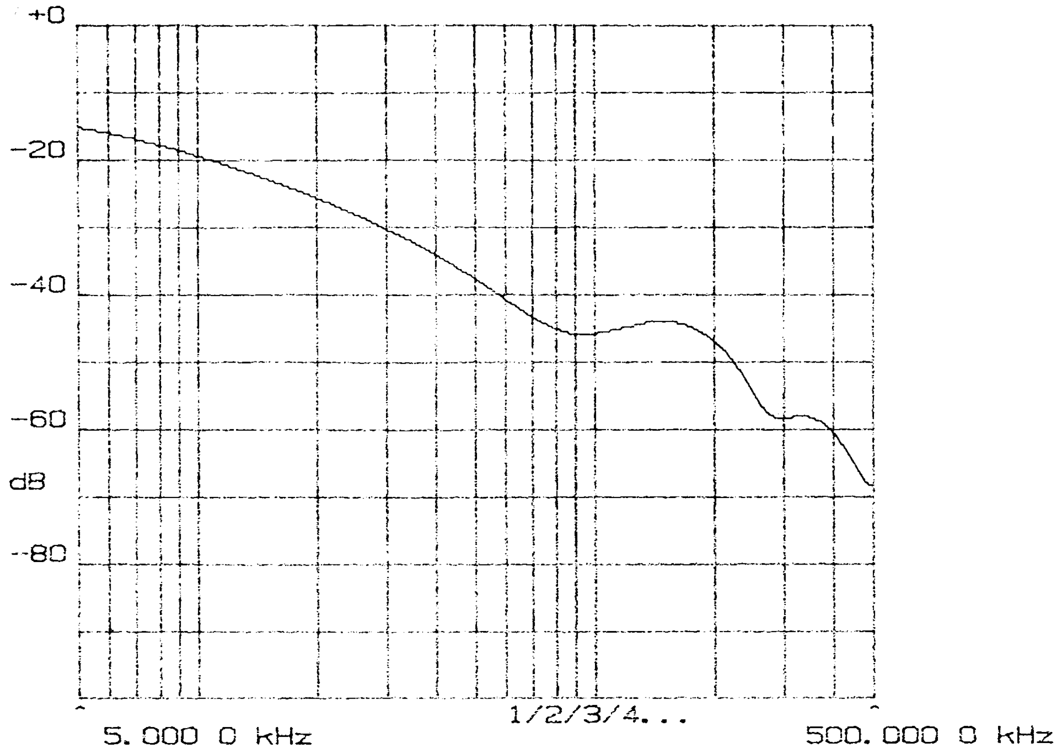


Figure C.15: Frequency response of loop 6

C.3.6 Frequency response of loop 7

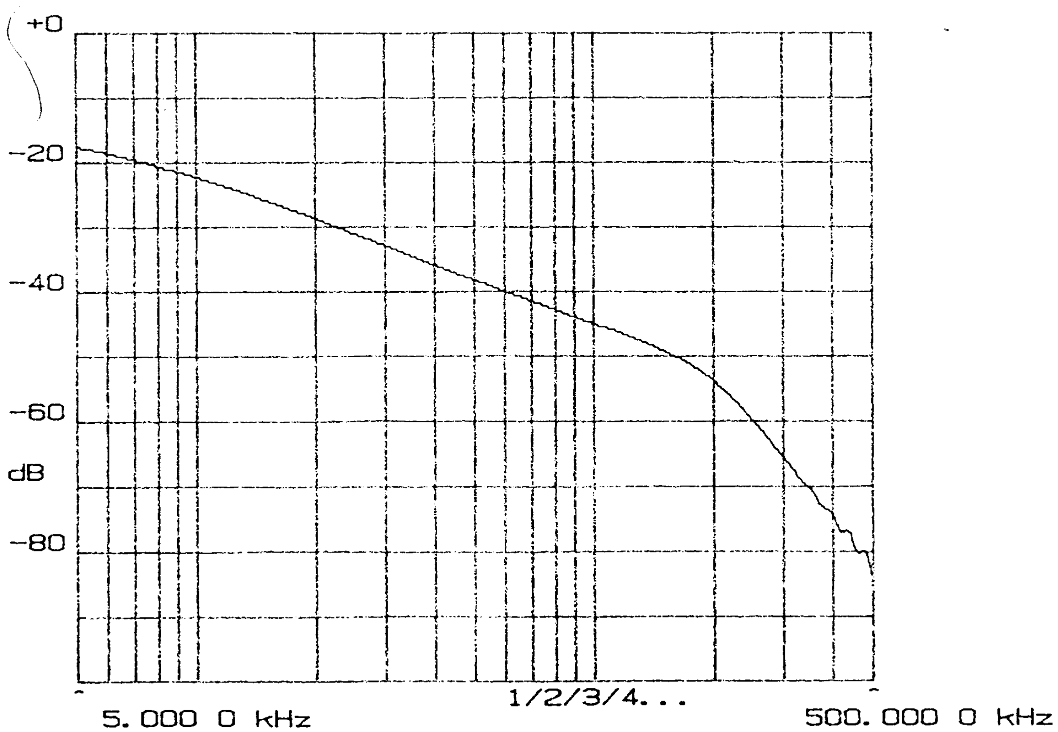


Figure C.16: Frequency response of loop 7

C.3.7 Frequency response of loop 8

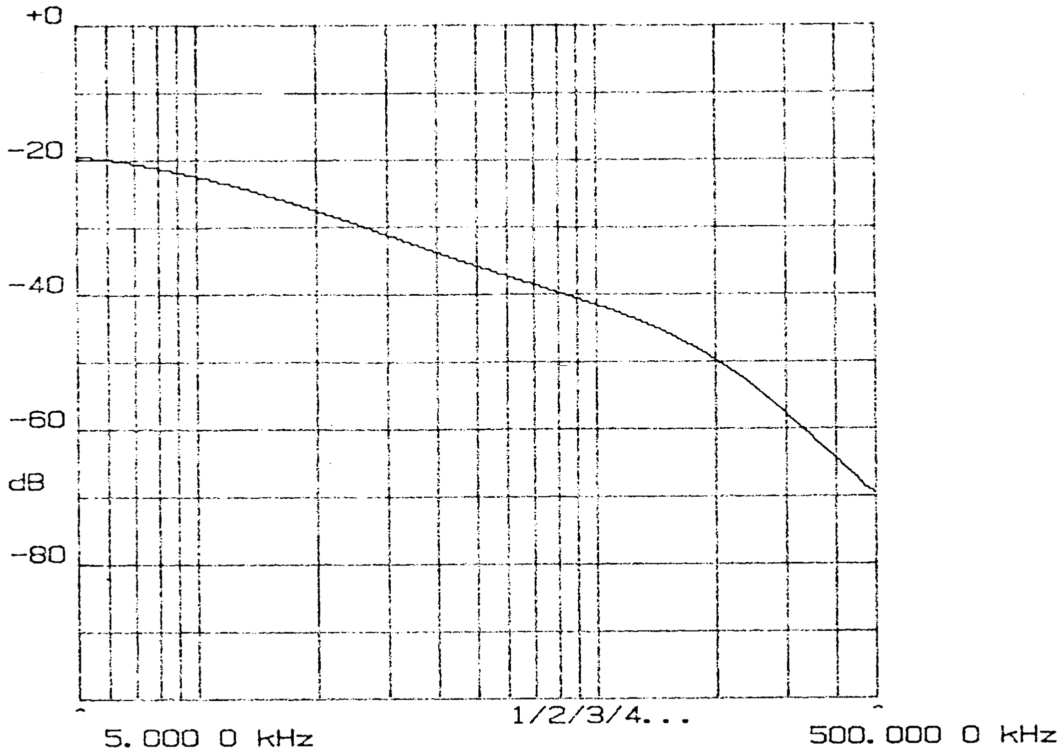


Figure C.17: Frequency response of loop 8

C.3.8 Frequency response loop 9

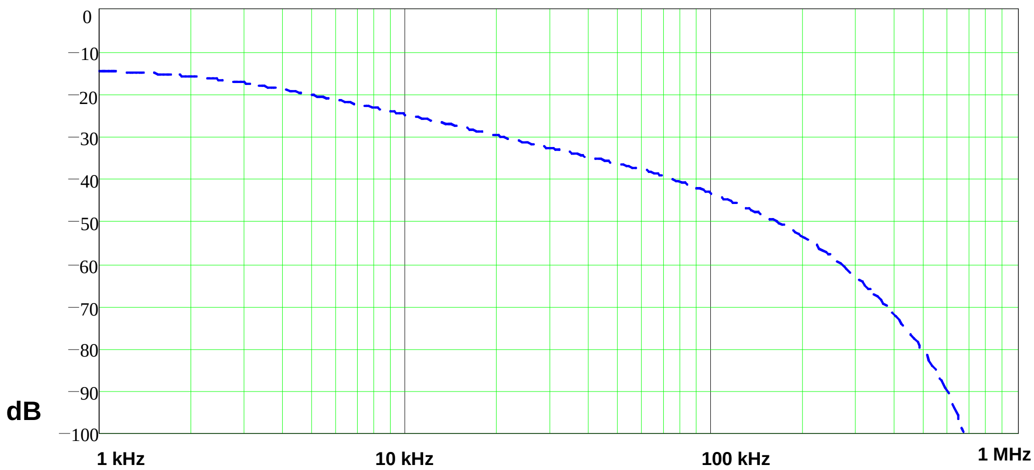


Figure C.18: Frequency response of loop 9

Bibliography

The following material, though not specifically referenced in the body of the present document (or not publicly available), gives supporting information.

Council Directive 73/23/EEC of 19 February 1973 on the harmonization of the laws of Member States relating to electrical equipment designed for use within certain voltage limits.

History

Document history		
V1.3.1	November 1998	Publication
V1.3.2	May 2000	Publication